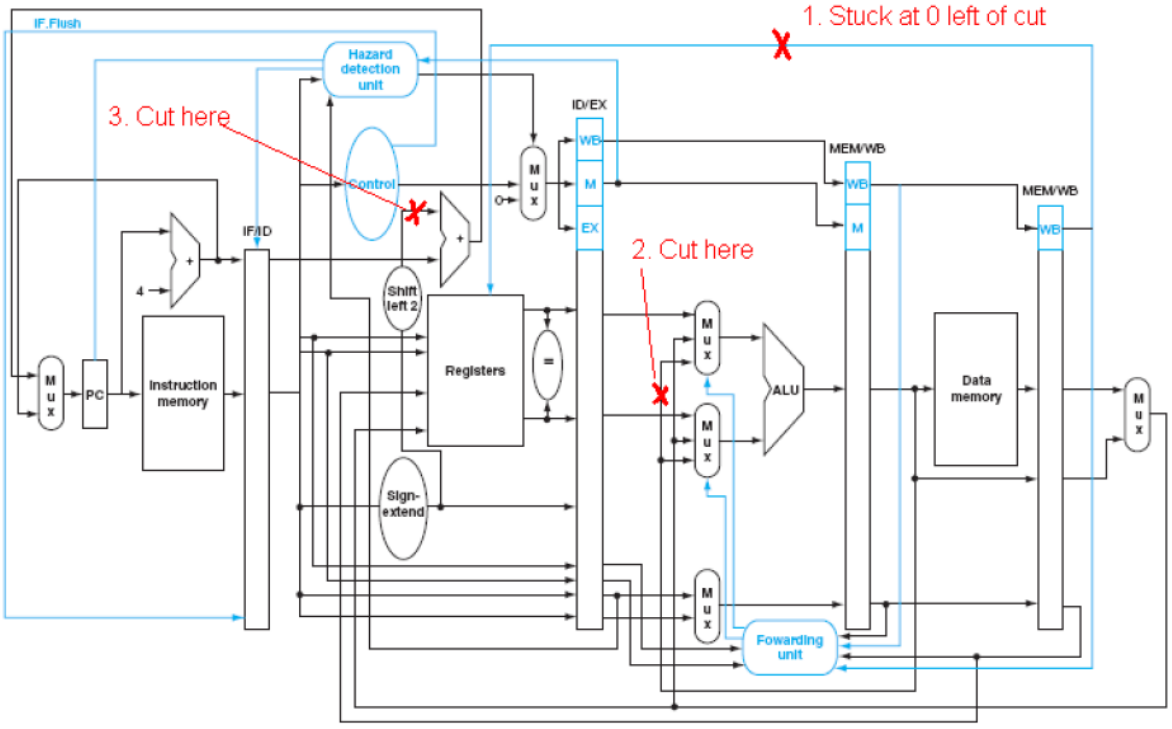
Home Task # 2
Computer System Architecture
No Submission

1. For the MIPS datapath shown below, several lines are marked with "X". For each one, describe in words the negative consequence of cutting this line relative to the working, unmodified processor.

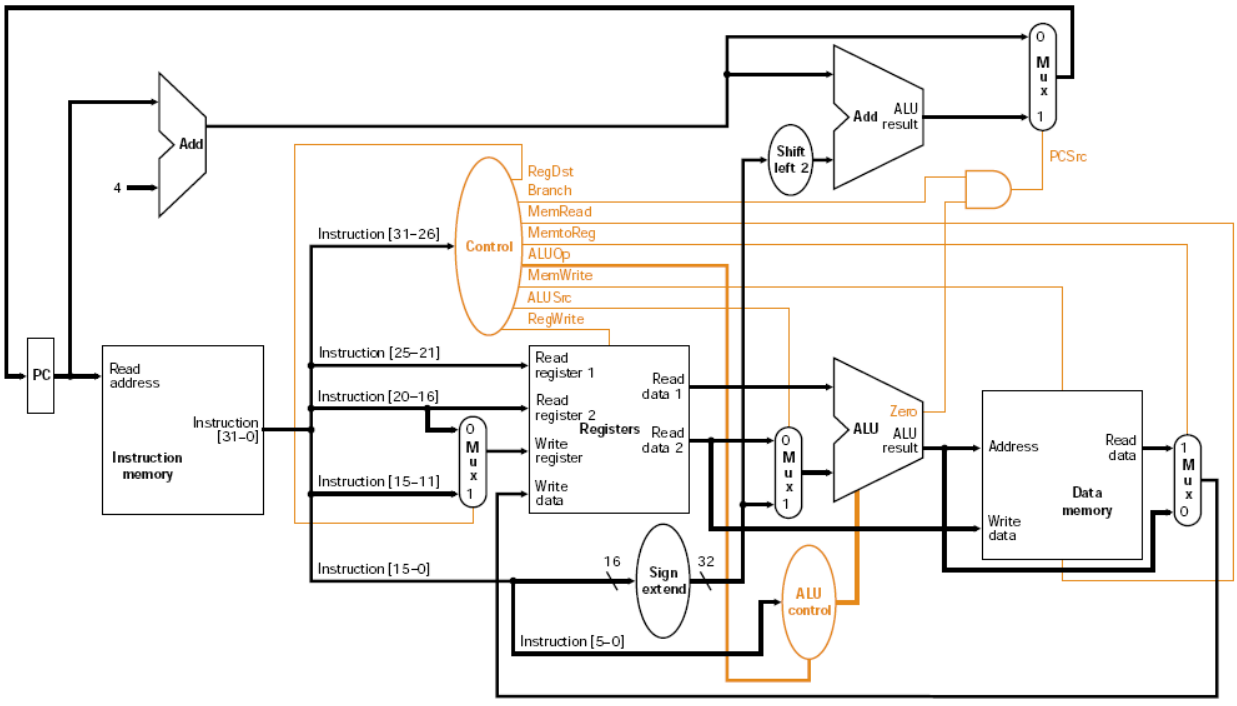


2. Structural, data and control hazards typically require a processor pipeline to stall. Listed below are a series of optimization techniques implemented in a compiler or a processor pipeline designed to reduce or eliminate stalls due to these hazards. For each of the following optimization techniques, state which pipeline hazards it addresses and how it addresses it. Some optimization techniques may address more than one hazard, so be sure to include explanations for all addressed hazards.
   (a) Branch Prediction
   (b) Instruction Scheduling
   (c) delay slots
   (d) increasing availability of functional units (ALUs, adders etc)
   (e) caches

3. This is a three-part question about critical path calculation. Consider a simple singlecycle implementation of MIPS ISA. The operation times for the major functional components for this machine are as follows:

Component	Latency
ALU	10 ns
Adder	8 ns
ALU Control Unit	2 ns
Shifter	3 ns
Control Unit/ROM	4 ns
Sign/zero extender	3 ns
2-1 MUX	2 ns
Memory (read/write) (instruction or data)	15 ns
PC Register (read action)	1 ns
PC Register (write action)	1 ns
Register file (read action)	7 ns
Register file (write action)	5 ns
Logic (1 or more levels of gates)	1 ns

Below is a copy of the MIPS single-cycle datapath design. In this implementation the clock cycle is determined by the longest possible path in the machine. The critical paths for the different instruction types that need to be considered are: R-format, Load-word, and store-word. All instructions have the same instruction fetch and decode steps.



a. In the table below, indicate the components that determine the critical path for the respective instruction, in the order that the critical path occurs. If a component is used, but not part of the critical path of the instruction (ie happens in parallel with another component), it should not be in the table. The register file is used for reading and for writing; it will appear twice for some instructions. All instruction begin by reading the PC register. **Note that, you are asked to tell about the elements used not the typical instruction stages.**

Instruction Type	Hardware Elements Used By Instruction											
R-Format												
Load												
Store												

b. Place the latencies of the components that you have decided for the critical path of each instruction in the table below. Compute the sum of each of the component latencies for each instruction.

Instruction Type	Hardware Latencies For Respective Elements											Total
R-Format	2 ns											
Load	2 ns											
Store	2 ns											

c. Use the total latency column to derive the following critical path information:

- Given the data path latencies above, which instruction determines the overall machine critical path (latency)?
- What will be the resultant clock cycle time of the machine based on the critical path instruction?
- What frequency will the machine run?

Chapter 3
Assignement-2 and Exercise questions
3.7, 3.8, 3.13, 3.28-3.33