

## Lecture 11a

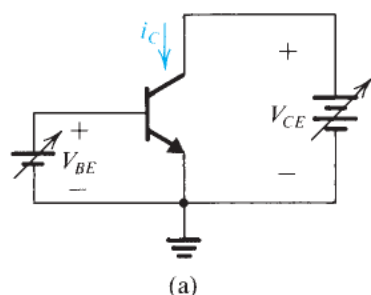
### EE-215 Electronic Devices and Circuits

Asst Prof Muhammad Anis Chaudhary

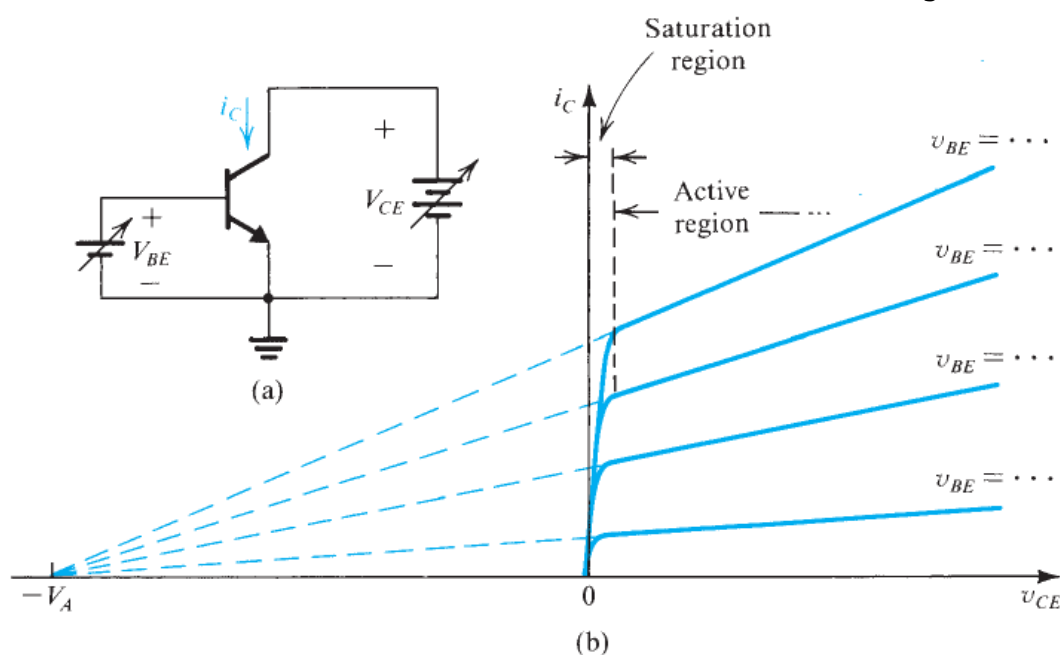
## BJT: Current-Voltage Characteristics

### Dependence of $i_C$ on the Collector Voltage - The Early Effect

- Consider the conceptual circuit shown in fig
  - here the transistor is connected in common-emitter configuration
    - i.e. the emitter acts as a common terminal between the input and output ports
    - the voltage  $V_{BE}$  can be set to any desired value

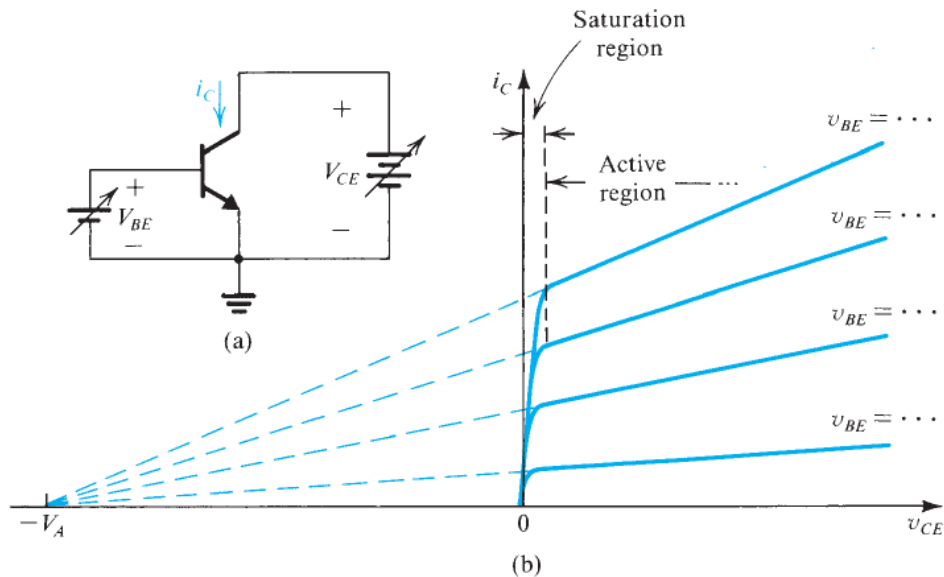


- for each value of  $V_{BE}$ , the corresponding  $i_C - v_{CE}$  characteristic curve can be measured point by point
  - by varying the dc voltage  $V_{CE}$  and measuring the corresponding  $i_C$
- the resulting family of  $i_C - v_{CE}$  characteristic curves are known as “common-emitter characteristics” and are shown in figure below

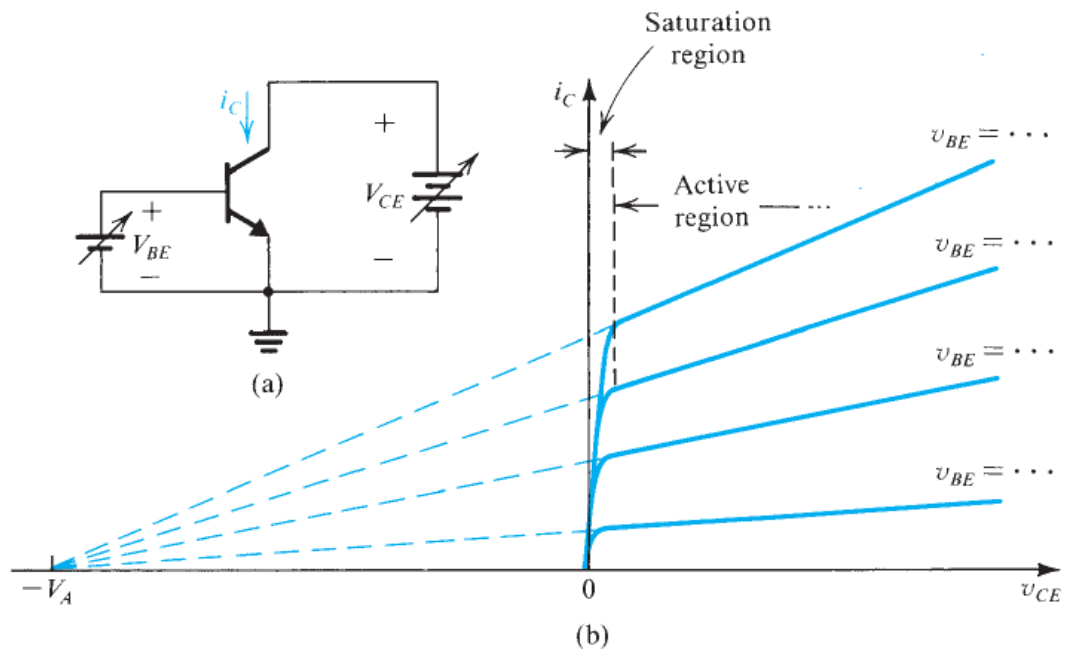


- it is clear from fig,





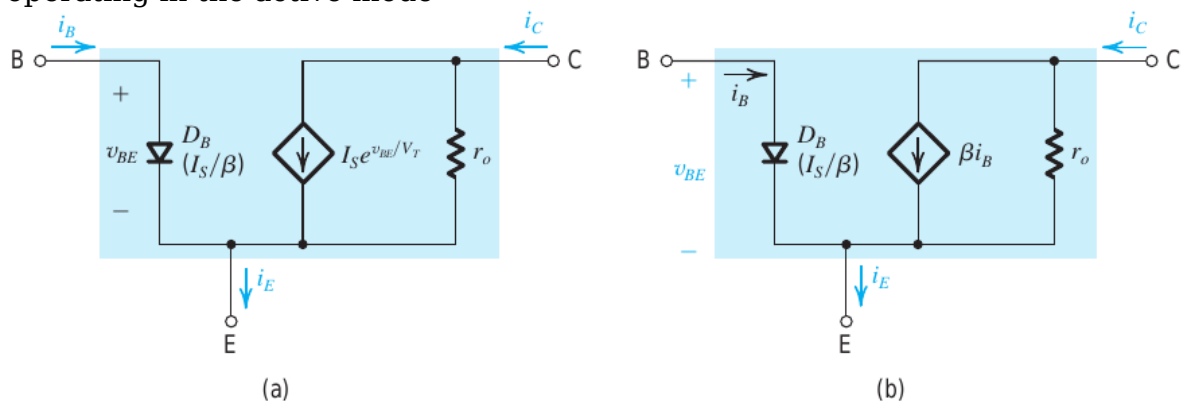
- when extrapolated, the characteristic lines meet at a point on the negative  $v_{CE}$  axis, at  $v_{CE} = -V_A$
- This voltage  $V_A$  is a positive number and is called Early voltage



- $V_A$  is a parameter for the particular BJT, and typically lies in the range of 10V to 100V
- Consider the extrapolated lines shown in fig
  - using the straight line equation  $y - y_1 = m(x - x_1)$ 
    - here  $y = i_C$ ,  $x = v_{CE}$ ,  $(x_1, y_1) = (-V_A, 0)$ ,  $(x_2, y_2) = (0.3, I_C')$
    - where  $I_C'$  is the value of the collector current with the Early effect neglected
- using the straight line equation  $y - y_1 = m(x - x_1)$ 
  - here  $y = i_C$ ,  $x = v_{CE}$ ,  $(x_1, y_1) = (-V_A, 0)$ ,  $(x_2, y_2) = (0.3, I_C')$ 
    - where  $I_C'$  is the value of the collector current with the Early effect neglected
    - $m = \frac{y_2 - y_1}{x_2 - x_1} = \frac{I_C' - 0}{0.3 - (-V_A)} = \frac{I_C'}{0.3 + V_A}$

- thus  $y - y_1 = m(x - x_1) \Rightarrow i_C - 0 = \frac{I_C'}{0.3+V_A} (v_{CE} - (-V_A))$
- or  $i_C = \frac{I_C'}{0.3+V_A} (v_{CE} + V_A)$
- As  $V_A > 0.3 \Rightarrow 0.3 + V_A \approx V_A$  ( $\because$  typically  $V_A = 10V$  to  $100V$ )
- $\Rightarrow i_C \approx \frac{I_C'}{V_A} (v_{CE} + V_A) = \frac{I_C'}{V_A} v_{CE} + \frac{I_C'}{V_A} V_A = \frac{I_C'}{V_A} v_{CE} + I_C'$
- or  $i_C = I_C' + \frac{I_C'}{V_A} v_{CE} = I_C' \left( 1 + \frac{v_{CE}}{V_A} \right)$
- $i_C = I_C' \left( 1 + \frac{v_{CE}}{V_A} \right) = I_S e^{v_{BE}/V_T} \left( 1 + \frac{v_{CE}}{V_A} \right)$
- $i_C = I_S e^{v_{BE}/V_T} \left( 1 + \frac{v_{CE}}{V_A} \right)$ 
  - the nonzero slope of the  $i_C - v_{CE}$  straight lines indicates that
    - the output resistance looking into the collector is not infinite.
  - Rather it is finite and is defined as
    - $r_o = \left[ \frac{\partial i_C}{\partial v_{CE}} \Big|_{v_{BE}=\text{constant}} \right]^{-1}$
  - substituting  $i_C = I_S e^{v_{BE}/V_T} \left( 1 + \frac{v_{CE}}{V_A} \right)$  into this relation
  - $r_o^{-1} = \frac{\partial i_C}{\partial v_{CE}} \Big|_{v_{BE}=\text{constant}} = \frac{\partial}{\partial v_{CE}} \left\{ I_S e^{v_{BE}/V_T} \left( 1 + \frac{v_{CE}}{V_A} \right) \right\} \Big|_{v_{BE}=\text{constant}}$
  - $r_o^{-1} = I_S e^{v_{BE}/V_T} \frac{\partial}{\partial v_{CE}} \left( 1 + \frac{v_{CE}}{V_A} \right) = I_C' \frac{\partial}{\partial v_{CE}} \left( 1 + \frac{v_{CE}}{V_A} \right)$
- $r_o^{-1} = I_C' \frac{\partial}{\partial v_{CE}} \left( 1 + \frac{v_{CE}}{V_A} \right) = I_C' \left( 0 + \frac{1}{V_A} \right) = \frac{I_C'}{V_A}$ 
  - $r_o = \frac{V_A}{I_C'}$
  - where  $I_C'$  is the value of the collector current with the Early effect neglected
    - i.e.  $I_C' = I_S e^{V_{BE}/V_T}$
  - it is rarely necessary to include the dependence of  $i_C$  on  $v_{CE}$  in dc bias design and analysis that is performed by hand.
  - The output resistance  $r_o$  can be easily included in the circuit model of the transistor

- fig shows the large-signal circuit models of a common-emitter npn transistor operating in the active mode



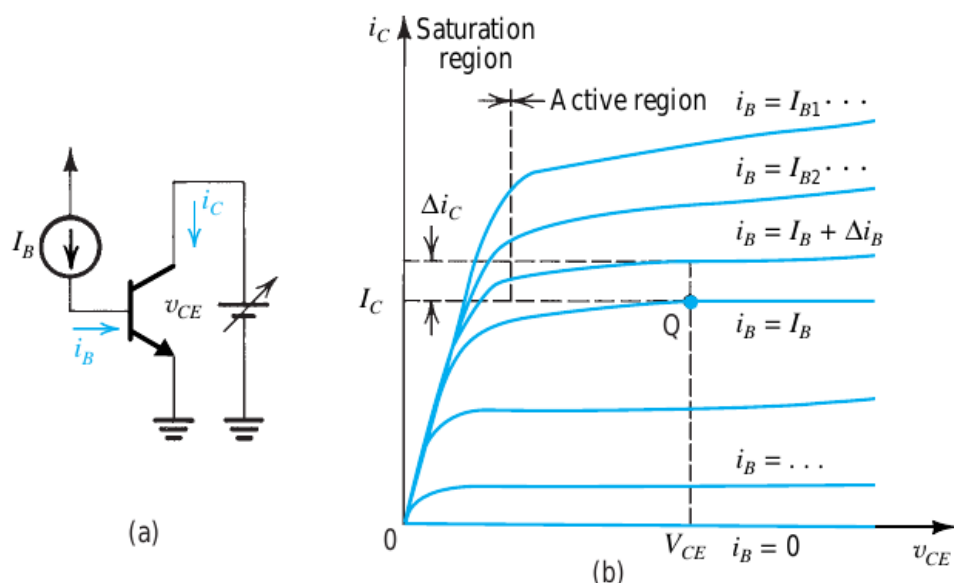
**Figure 6.18** Large-signal equivalent-circuit models of an npn BJT operating in the active mode in the common-emitter configuration with the output resistance  $r_o$  included.

- Note that here the resistance  $r_o$  is connected between the collector and the emitter terminals

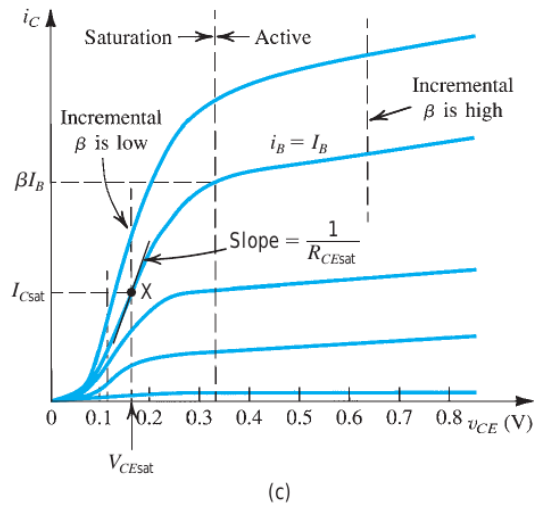
## BJT: Current-Voltage Characteristics

### An Alternative Form of the Common-Emitter Characteristics

- An alternative way of expressing the transistor common-emitter characteristics is shown in fig

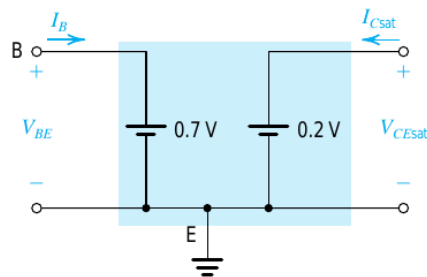


- here the base current  $i_B$  rather than  $v_{BE}$  is used as a parameter
  - i.e. each  $i_C - v_{CE}$  curve is measured with the base fed with a constant current  $I_B$
- the expanded view of the common emitter characteristics in the saturation region is shown in figure
  - Note that the  $i_C - v_{CE}$  curves in the saturation region are rather steep,
    - $\Rightarrow$  the saturated transistor exhibits a low collector-to-emitter resistance  $R_{CEsat}$ 
      - $R_{CEsat} = \left. \frac{\partial v_{CE}}{\partial i_C} \right|_{i_B = I_B, i_C = I_{Csat}}$
      - typically,  $R_{CEsat}$  ranges from a few ohms to a few tens of ohms



- A simple model for the saturated BJT utilizing the constant voltage drop model for EBJ and CBJ can be given as

- here  $V_{BE}$  is assumed constant i.e.  $V_{BE} \approx 0.7V$ 
  - as  $V_{BE}$  ranges from 0.6V-0.8V
  - and  $V_{CE}$  also is assumed constant, i.e.  $V_{CE(sat)} \approx 0.2V$ 
    - as  $V_{CE}$  ranges from 0.1-0.3V



**Figure 6.20** A simplified equivalent-circuit model of the saturated transistor.

- Note that here we have neglected the small saturation resistance  $R_{CE(sat)}$ , to make the model simple for hand calculations

## BJT Circuits at DC

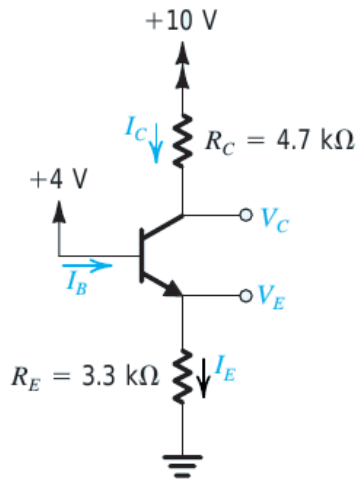
- to analyze the BJT circuits, to which only dc voltages are applied,
  - we will use the simple model in which
    - $|V_{BE}|$  of a conducting transistor is 0.7V
    - and  $|V_{CE}|$  of a saturated transistor is 0.2 V
  - we can neglect the Early effect in dc analysis
  - In analyzing a circuit, the first question that one must answer
    - is In which mode is the transistor operating?
  - based upon the terminal voltages, one need to determine whether the BJT is cutoff or conducting
  - if the tranistor is conducting,
    - we need to determine whether it is operating in the active mode or in saturation
- if it is not clear whether the BJT is in active mode or saturation, proceed as follows

- Assume the transistor is in active mode
  - determine the various voltages and currents
  - then check for consistency of the results with the assumption of active-mode operation
  - i.e.  $v_{CB} > -0.4$  for an npn and  $v_{BC} > -0.4$  for a pnp
  - if the answer is yes, then our task is complete.
  - otherwise assume saturation mode operation and proceed with the analysis
- Note that to test the validity of the assumption of saturation-mode operation,
  - one can compute the ratio  $I_C/I_B$  and verify if this ratio is lower than  $\beta$  i.e.  $\beta_{forced} < \beta$
  - As  $\beta$  for a given transistor varies over a wide range, use the lowest specified  $\beta$  for this test.

Table 6.3 Conditions and Models for the Operation of the BJT in Various Modes		
	npn	pnp
<b>Cutoff</b> EJB: Reverse Biased CBJ: Reverse Biased		
<b>Active</b> EJB: Forward Biased CBJ: Reverse Biased		
<b>Saturation</b> EJB: Forward Biased CBJ: Forward Biased		

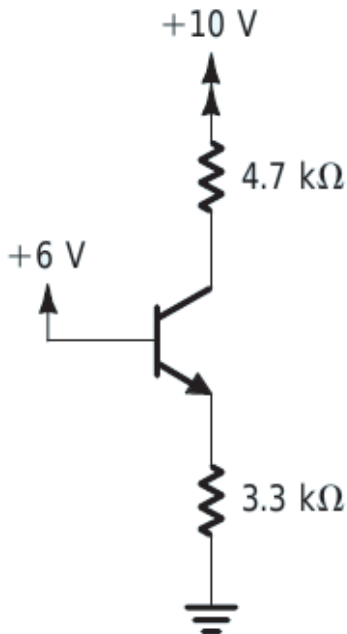
### Example 6.4

- Consider the circuit shown in Fig. 6.22(a). We wish to analyze this circuit to determine all node voltages and branch currents. We will assume that  $\beta$  is specified to be 100.



**Example 6.5**

- We wish to analyze the circuit of Fig. 6.23(a) to determine the voltages at all nodes and the currents through all branches. Note that this circuit is identical to that of Fig. 6.22 except that the voltage at the base is now +6 V. Assume that the transistor  $\beta$  is specified to be at least 50.

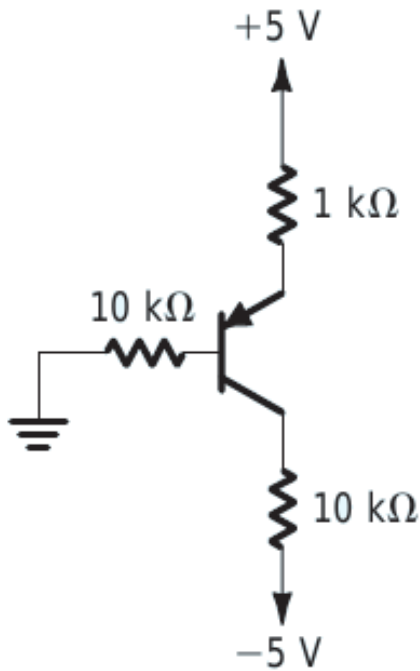


**Example 6.6**

**Example 6.9**

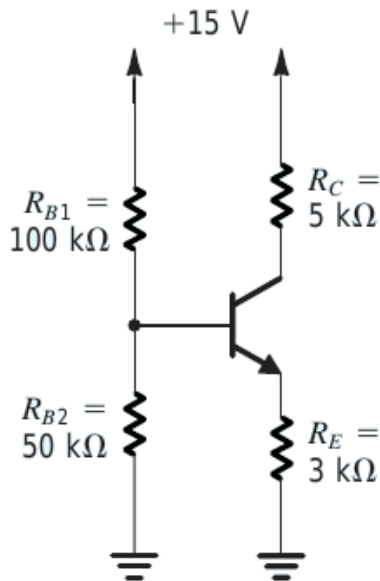
- We want to analyze the circuit of Fig. 6.27(a) to determine the voltages at all nodes and the currents through all branches. The minimum value of  $\beta$  is specified to be 30.





**Example 6.10**

- We want to analyze the circuit of Fig. 6.28(a) to determine the voltages at all nodes and the currents through all branches. Assume  $\beta = 100$ .



**Example 6.11**

- We want to analyze the circuit in Fig. 6.29(a) to determine the voltages at all nodes and the currents through all branches. Assume  $\beta = 100$  for both transistors.

