Lecture 11b

EE-215 Electronic Devices and Circuits

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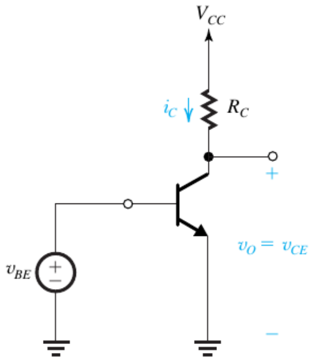
Applying the BJT in Amplifier Design

- When operated in active mode, the BJT functions as a voltage-controlled current source.
    - (i.e. the base-emitter voltage v_{BE} controls the collector current i_C)
    - this enables us to use the BJT in the design of amplifiers

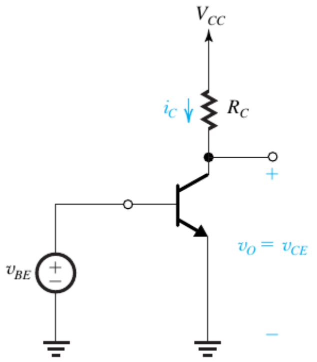
Obtaining a Voltage amplifier

- A voltage controlled current source can be used as a transconductance amplifier
    - A transconductance amplifier is an amplifier whose input signal is a voltage and output signal is a current
        - we usually are more interested in a voltage amplifier
    - A transconductance amplifier can be converted into a voltage amplifier,
        - by passing the output current through a resistor
        - and taking the voltage across the resistor as output

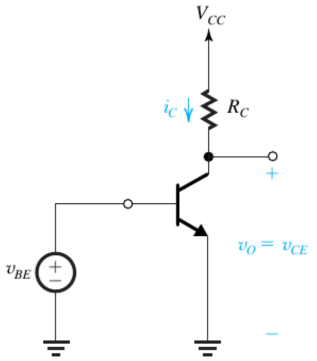


- in the figure
    - v_{BE} is the input voltage
        - R_C is called the load resistance.
            - R_C converts the collector current i_C to a voltage $i_C R_C$
            - V_{CC} is the supply voltage
        - here the output voltage is taken between the collector terminal and the ground (rather than across R_C)
            - this arrangement enables us to maintain a ground reference through out the circuit
            - $= \Rightarrow$

- v_{BE} is the input voltage
- v_{CE} is the output voltage

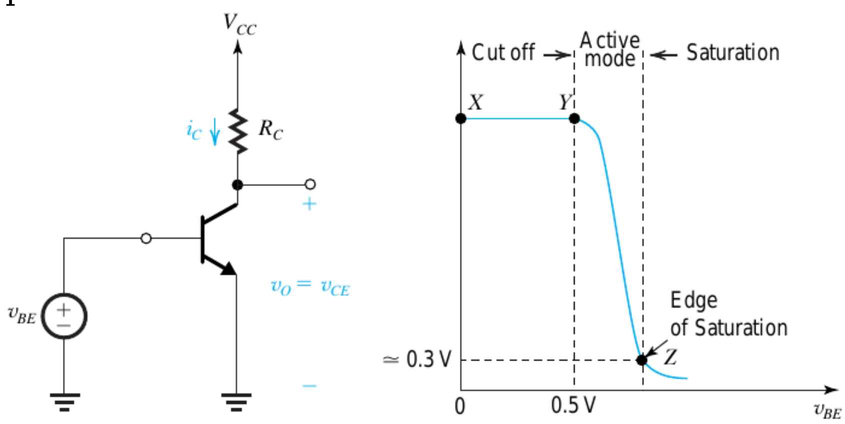


- Using KVL, an expression for v_{CE} can be computed
  - i.e. $V_{CC} = i_C R_C + v_{CE}$
    - or $v_{CE} = V_{CC} - i_C R_C$
    - $= \Rightarrow$ output voltage v_{CE} is an inverted version of $i_C R_C$ that is shifted by the constant value of the supply voltage V_{CC}



The Voltage Transfer Characteristic (VTC)

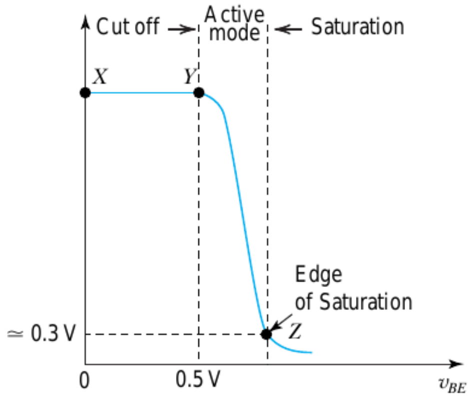
- VTC is a plot of the output voltage versus the input voltage
  - and it can provide a better insight in to the operation of an amplifier circuit



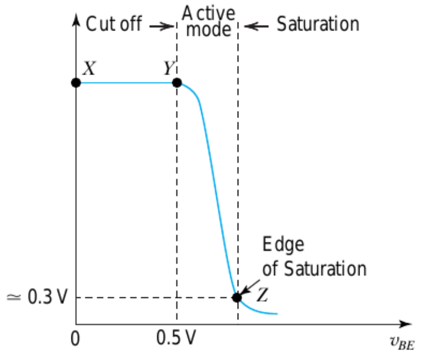
  - **Figure 6.31** **(a)** Simple BJT amplifier with input v_{BE} and output v_{CE}. **(b)** The voltage transfer characteristic (VTC) of the amplifier in **(a)**. The three segments of the VTC correspond to the three modes of operation of the BJT.

- Note that for $v_{BE} < 0.5V$, the transistor is cut-off $= \Rightarrow i_C = 0$

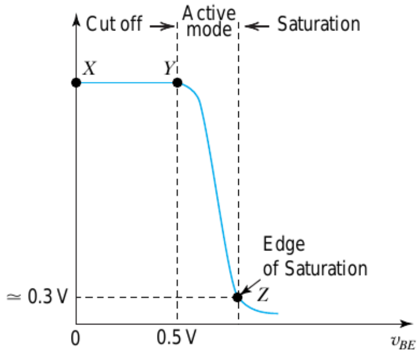
- and $v_{CE} = V_{CC} - i_C R_C = V_{CC} - (0)R_C = V_{CC}$
  - As v_{BE} exceeds $0.5V$, the transistor turns on and v_{CE} decreases.
    - As initially i_C is still small
    - $= \Rightarrow v_{CE}$ is still high
    - $= \Rightarrow$ BJT is operating in active region (active region: $v_{CE} \geq 0.3V$)



- BJT stays in active region as v_{BE} is increased
  - untill the value of v_{BE} is reached for which v_{CE} becomes lower than v_{BE} by 0.4 V i.e. $v_{CE} \approx 0.3V$
    - this is point Z



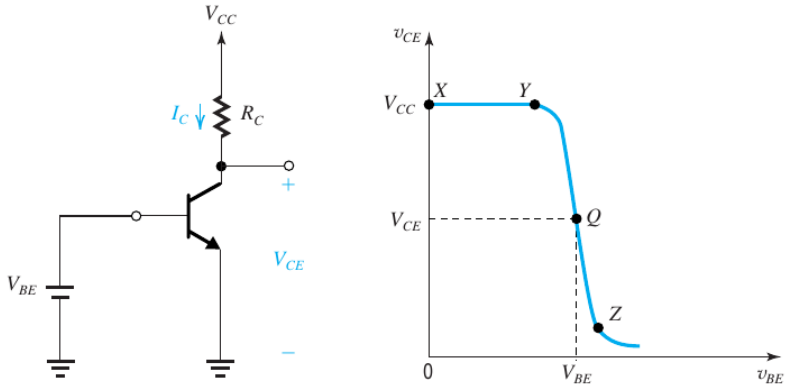
  - for $v_{CE} < 0.3V$ (i.e. beyond point Z), the transistor enters the saturation region,
- from the fig, it is clear that the segment of greatest slope
  - (and hence the largest amplifier gain) is that labeled as YZ
    - which corresponds to the active mode of operation
  - thus for amplifier application, one will always choose to operate the BJT in active mode



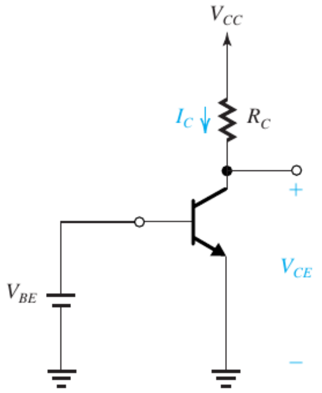
- thus for amplifier application, the BJT will be operated in active mode i.e. in the segment YZ
  - for active mode operation (ignoring base-width modulation or the Early Effect)
    - $i_C = I_S e^{v_{BE}/V_T}$
  - As $v_{CE} = V_{CC} - i_C R_C$
    - $= \Rightarrow v_{CE} = V_{CC} - \left(I_S e^{v_{BE}/V_T}\right) R_C$
  - $v_{CE} = V_{CC} - R_C I_S e^{v_{BE}/V_T}$
  - Although this is a non-linear relationship, but linear (or almost linear) amplification is possible,
    - by using the technique of biasing the BJT

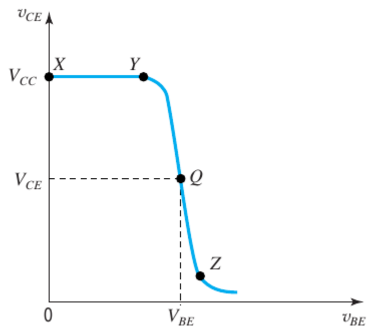
Biasing the BJT to Obtain Linear Amplification

- Biasing enables us to obtain almost-linear amplification from the BJT

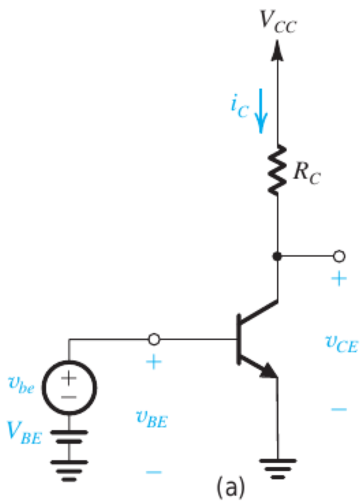


  - **Figure 6.32** Biasing the BJT amplifier at a point Q located on the active-mode segment of the VTC.
  - A dc voltage V_{BE} is selected to obtain operation at a point Q on the segment YZ
- the resulting V_{CE} can be given as
  - $V_{CE} = V_{CC} - R_C I_S e^{V_{BE}/V_T}$
    - Point Q is called the bias point
      - or the dc operating point
      - or the Quiescent point

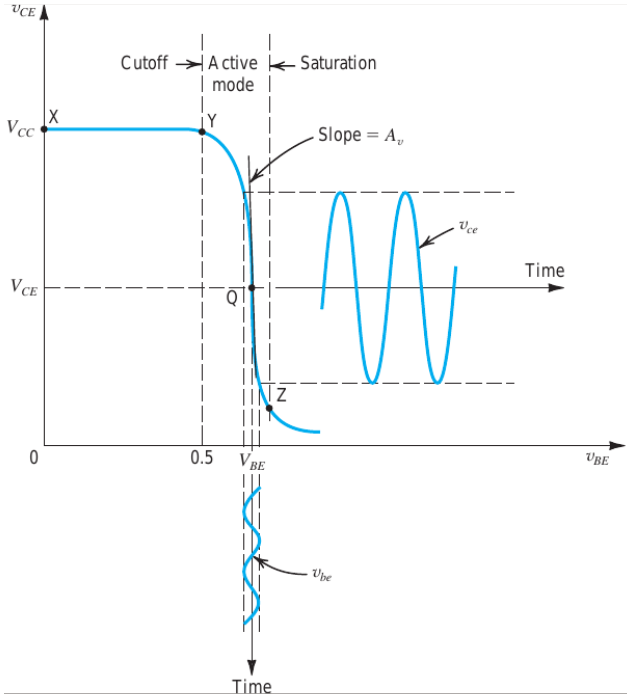




- Once the Q point is selected, the ac signal to be amplified is superimposed on the bias voltage V_{BE}
    - $= \Rightarrow$ the total instantaneous value of v_{BE} is
        - $v_{BE}(t) = V_{BE} + v_{be}(t)$
        - the resulting v_{CE} is
            - $v_{CE} = V_{CC} - R_C I_S e^{v_{BE}/V_T}$

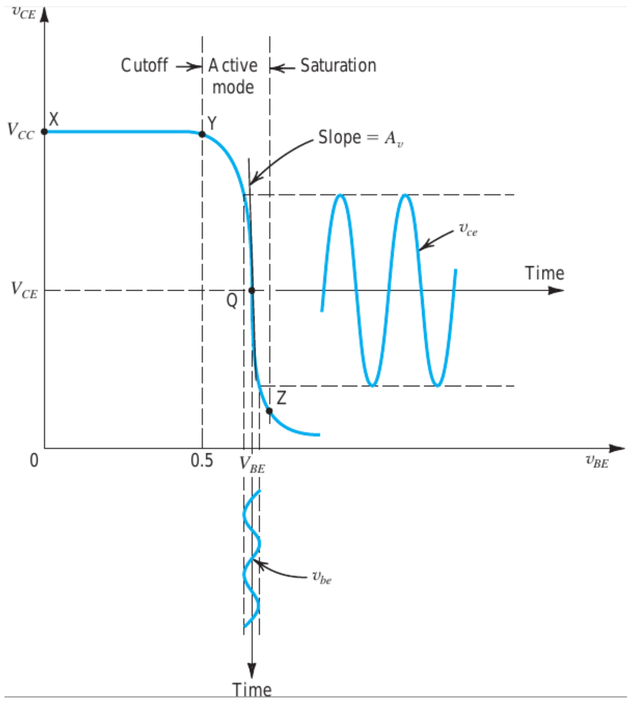


- $v_{CE}(t)$ can also be obtained graphically from the VTC
    - Note that if the amplitude of v_{be} is small enough to
        - restrict the signal swing to a short almost-linear segment
            - of the VTC, linear amplification is achieved
        - The shorter the segment, the greater the linearity achieved.

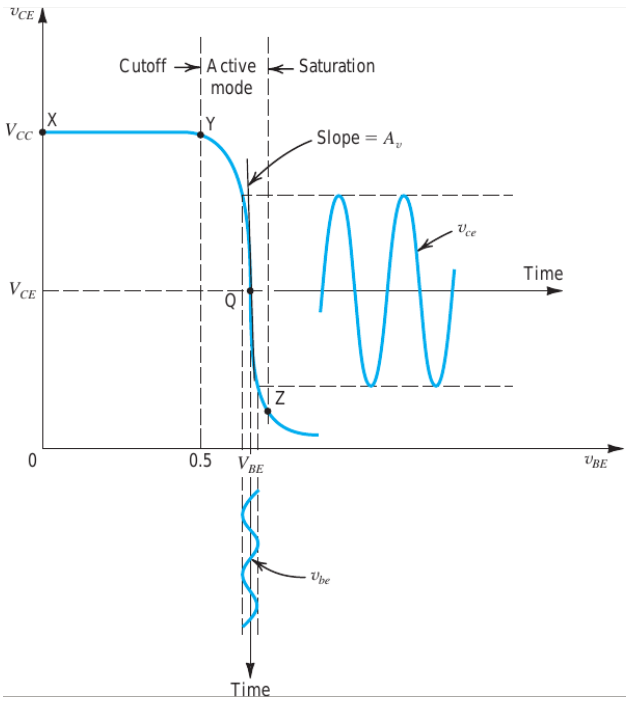


The Small-Signal Voltage Gain

- if the input signal v_{be} is kept small, the output signal v_{ce} is nearly proportional to v_{be}
  - i.e. $v_{ce} \propto v_{be}$
    - or $v_{ce} = A_v v_{be}$
    - A_v is the proportionality constant and is the voltage gain of the amplifier
    - A_v is the slope of the almost linear segment of the VTC around Q
      - i.e. $A_v = . \left.\frac{\partial v_{CE}}{\partial v_{BE}}\right|_{v_{BE}=V_{BE}}$



- $A_v = . \frac{\partial v_{CE}}{\partial v_{BE}}\Big|_{v_{BE}=V_{BE}}$
  - using $v_{CE} = V_{CC} - R_C I_S e^{v_{BE}/V_T}$
    - $A_v = . \frac{\partial}{\partial v_{BE}}\left[V_{CC} - R_C I_S e^{v_{BE}/V_T}\right]\Big|_{v_{BE}=V_{BE}}$
    - $A_v = . \left[0 - R_C I_S \frac{\partial}{\partial v_{BE}}\left(e^{v_{BE}/V_T}\right)\right]\Big|_{v_{BE}=V_{BE}}$
    - $A_v = . \left[-R_C I_S e^{v_{BE}/V_T} \frac{\partial}{\partial v_{BE}}\left(v_{BE}/V_T\right)\right]\Big|_{v_{BE}=V_{BE}}$
    - $A_v = . \left[-\frac{R_C I_S}{V_T} e^{v_{BE}/V_T}\right]\Big|_{v_{BE}=V_{BE}}$
    - $A_v = -\frac{R_C I_S}{V_T} e^{V_{BE}/V_T} = -\frac{R_C}{V_T} I_S e^{V_{BE}/V_T}$
    - $A_v = -\frac{R_C}{V_T} I_C \because I_C = I_S e^{V_{BE}/V_T}$
    - $= \Rightarrow A_v = -\frac{I_C}{V_T} R_C$
- $A_v = -\frac{I_C}{V_T} R_C$
  - from this expression, Note that
    1. The voltage gain is negative
       - $= \Rightarrow$the amplifier is inverting.
       - i.e . there is a 180^o phase shift between the input and the output
       - this inversion is clear from the figure
    2. The gain is proportional to the load resistance R_C,
       - and to the collector bias current I_C



- $A_v = -\frac{I_C}{V_T} R_C$

- $A_v = -\frac{I_C R_C}{V_T} = -\frac{V_{RC}}{V_T}$
    - where V_{RC} is the dc voltage drop across R_C i.e. $V_{RC} = V_{CC} - V_{CE}$
- thus the gain is simply the ratio of the dc voltage drop across the load resistor R_C
    - to the thermal voltage V_T ($\approx 25mV$ at room temperature)
- this relation is useful in determining the absolute upper limit on the magnitude of voltage gain for this amplifier circuit

- Note that
    - the theoretical maximum gain A_v is obtained by biasing the BJT at the edge of saturation,
        - (which would not leave any room for negative signal swing)
        - The resulting gain can be given as
        - $A_v = -\frac{V_{RC}}{V_T} = -\frac{V_{CC}-V_{CE}}{V_T} = -\frac{V_{CC}-0.3}{V_T} \because V_{CE} = 0.3$ at edge of saturation
        - As $V_{CC} - 0.3 \approx V_{CC}$
    - $A_{vmax} \approx -\frac{V_{CC}}{V_T}$ or $\left|A_{vmax}\right| \approx \frac{V_{CC}}{V_T}$

Determining the VTC by Graphical Analysis

- Voltage transfer characteristic (VTC) of the amplifier can be determined using graphical method

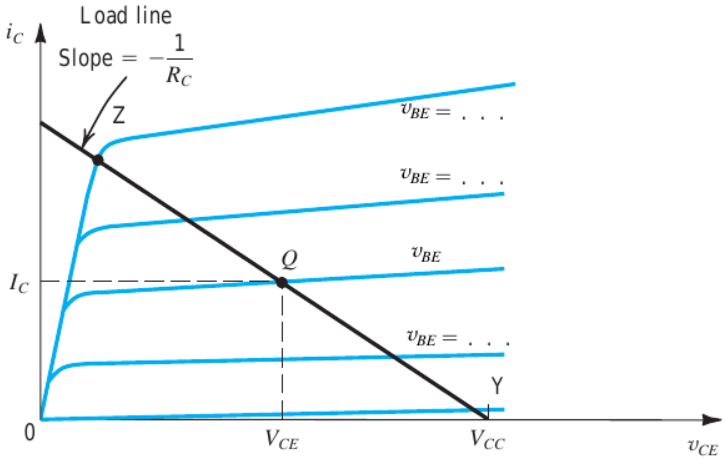
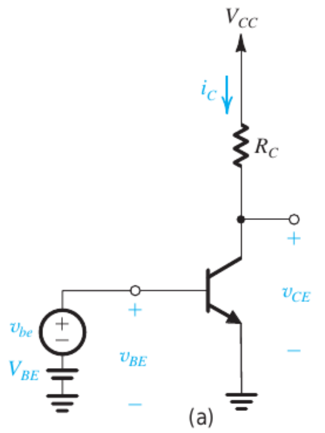
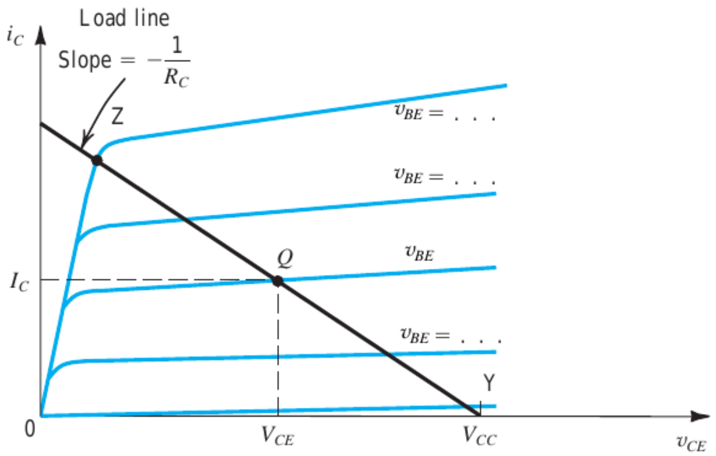


Figure 6.34 Graphical construction for determining the VTC of the amplifier circuit of Fig. 6.33(a).





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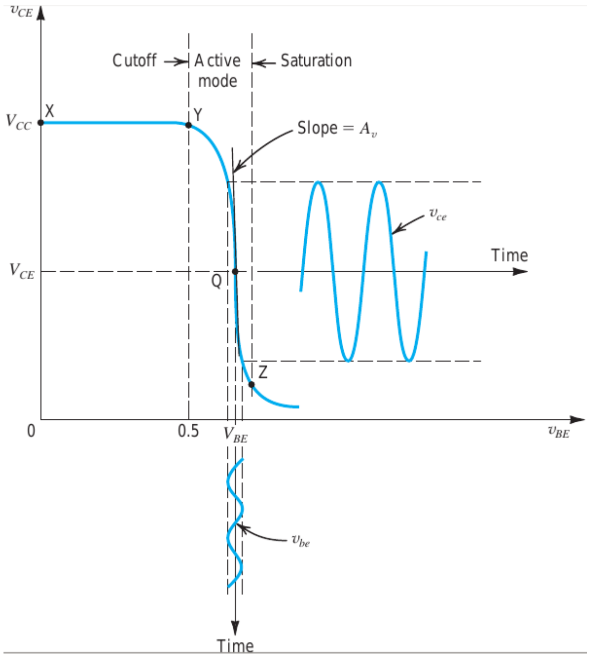


- the graphical analysis is based on the fact that
  - for each value of v_{BE}, the circuit will be operating
    - at the point of intersection of the $i_C - v_{BE}$ graph
      - corresponding to that particular value of v_{BE}
      - and the straight line representing the KVL eq
      - i.e. $v_{CE} = V_{CC} - R_C i_C \implies i_C = \frac{V_{CC}}{R_C} - \frac{v_{CE}}{R_C}$

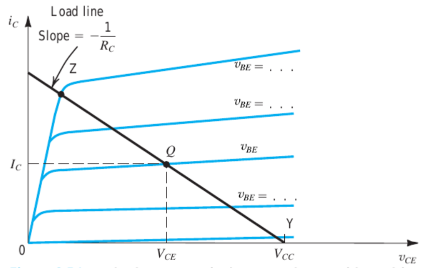


Figure 6.34 Graphical construction for determining the VTC of the amplifier circuit of Fig. 6.33(a).

- The straight line representing this relationship is superimposed on the $i_C - v_{CE}$ characteristic
- this line intersects the horizontal axis at $v_{CE} = V_{CC}$ and has a slope of $-\frac{1}{R_C}$
  - this line is called the load line as it represents the load resistance R_C
    - the VTC can then be determined point by point
      - here three important points have been labeled
    - At point Y
      - $v_{BE} = 0.5V$ (cutin voltage of EBJ)
    - At point Q
      - BJT can be biased for amplifier application i.e. $v_{BE} = V_{BE}$, $v_{CE} = V_{CE}$

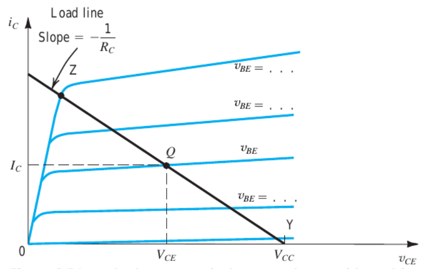
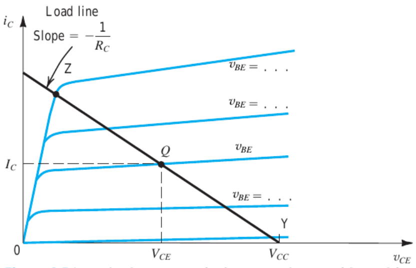


Figure 6.34 Graphical construction for determining the VTC of the amplifier circuit of Fig. 6.33(a).

- At point Z,
  - the BJT leaves the active region and enters the saturation region
    - Note that if the BJT is to be used as a switch, then operating points Y and Z are applicable
      - At Y, the transistor is off (open switch)
      - and at Z the transistor operates as a low valued resistance R_{CEsat} and has a small voltage drop (closed switch)



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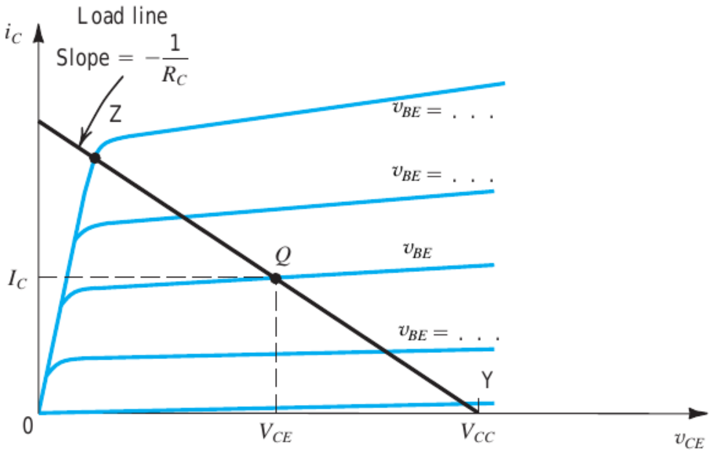

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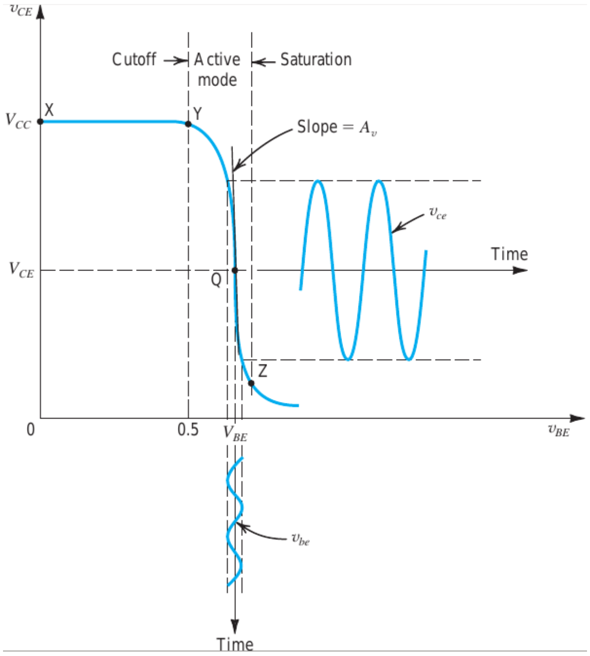


Locating the Bias Point Q

- The bias point Q is determined by the value of v_{BE} and that of the load resistance R_C
  - Two important considerations in choosing the location of Q are
    - the required gain and
      - the allowable signal swing at the output

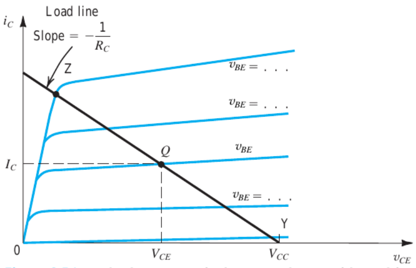
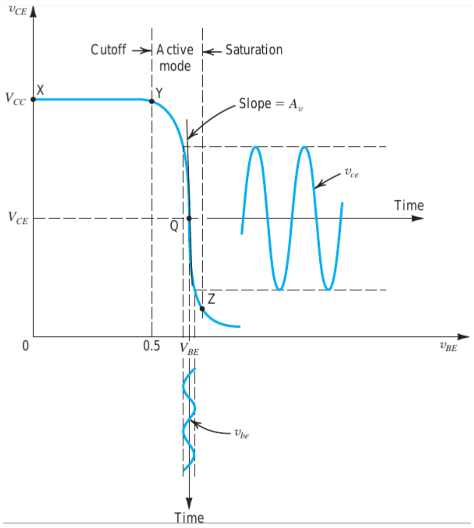
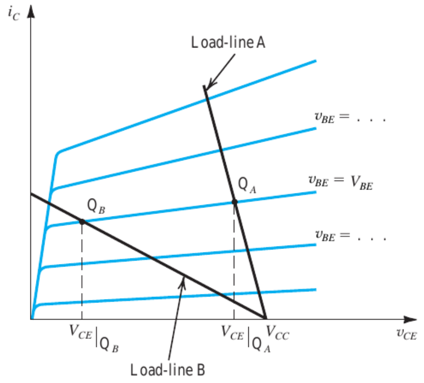


Figure 6.34 Graphical construction for determining the VTC of the amplifier circuit of Fig. 6.33(a).

- Consider the VTC shown in figure
  - here the value of R_C is fixed
    - the only remaining variable is the value of V_{BE}
    - Note that the slope increases as we move closer to point Z
      - thus higher gain is achieved by locating Q as close to Z as possible
    - However the closer Q is to the boundary point Z,
      - the smaller the allowable magnitude of negative signal swing



- to decide on the value of R_C, $i_C - v_{CE}$ plane is useful
  - here two load lines are shown which result in two exreme bias points
    - Point Q_A is too close to V_{CC}
      - resulting in a severe constaint on the positive signal swing of v_{ce}
      - Exceeding the allowable +ve maximum will result in positive peaks of the signal being cliiped off,
      - since the BJT will turn off for the part of each cycle near the+ve peak
      - we say the circuit doesnot have sufficient "headroom"



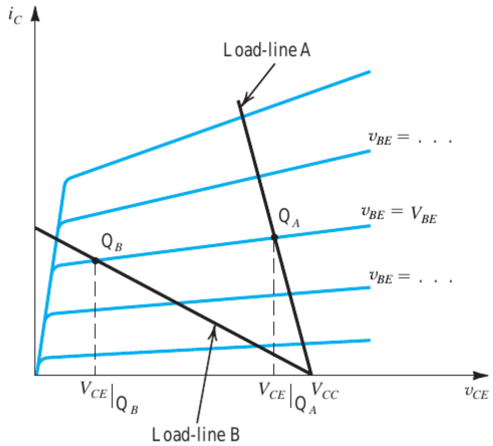
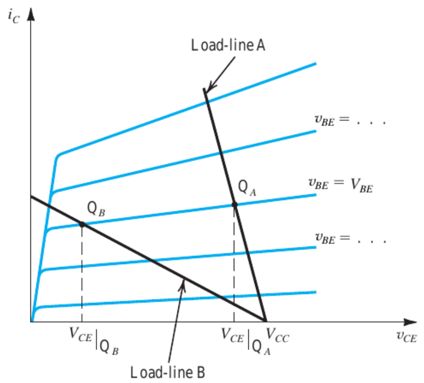


Figure 6.35 Effect of bias-point location on allowable signal swing: Load line A results in bias point Q$_A$ with a corresponding V_{CE} that is too close to V_{CC} and thus limits the positive swing of v_{CE}. At the other extreme, load line B results in an operating point, Q$_B$, too close to the saturation region, thus limiting the negative swing of v_{CE}.

- Point Q_B is very close to the boundary of the saturation region,
  - thus severely limiting the allowable negative signal swing of v_{ce}
    - Exceeding this limit results in the transistor entering the saturation region,
      - for part of each cycle near the negative peaks,
      - resulting in a distorted output signal
      - we say the circuit doesnot have sufficient "legroom"



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