Lecture 14

EE-215 Electronic Devices and Circuits

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Biasing in BJT Amplifier Circuits

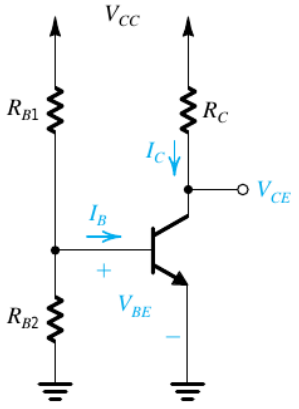
- we have already determined
  - In the design of a BJT amplifier circuit,
    - it is essential to establish an appropriate dc operating point (or Q point or bias point) for the BJT
    - This step is known as biasing or bias design
  - An appropriate bias point or dc operating point is characterized by
    - a stable and predictable dc collector current I_C and
    - by a dc collector-to-emitter voltage V_{CE} that ensures operation in the active region for all expected input signal levels

Biasing by Fixing V_{BE} or Biasing by Fixing I_B

- Two obvious schemes for biasing the BJT are
  1. Biasing by fixing V_{BE}
  2. Biasing by fixing I_B
  - Both these schemes result in wide variations in I_C and hence in V_{CE}
  - and are therefore not recomended for practical amplifiers

Biasing by Fixing V_{BE}

- in this case BJT is biased by fixing its V_{BE}
  - This voltage V_{BE} can be easily derived from the power-supply V_{CC}
    - by using an appropriate voltage divider
    - however, this way of biasing a BJT is not a viable approach
      - because the very sharp exponetial relationship $i_C - v_{BE}$ means that any small and inevitable differences in V_{BE} from the desired value will result in large differences in I_C and in V_{CE}
    - $I_C = I_S e^{V_{BE}/V_T}$,
    - $V_{CC} = I_C R_C + V_{CE} = \Rightarrow V_{CE} = V_{CC} - I_C R_C$

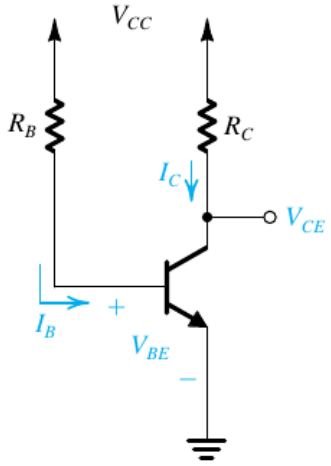


(a)

Biasing by Fixing I_B

- in this case BJT is biased by establishing a constant current in the base, I_B
  - here by ohms' law

- $I_B = \frac{V_{CC} - V_{BE}}{R_B} \approx \frac{V_{CC} - 0.7}{R_B} \because V_{BE} \approx 0.7V$
- again this is not a recommended approach
- because typically large variations in the value of β exist among units of the same device type
- this variation in β will result in large variation in I_C (as $I_C = \beta I_B$)
- and hence in V_{CE} (as $V_{CE} = V_{CC} - I_C R_C$)



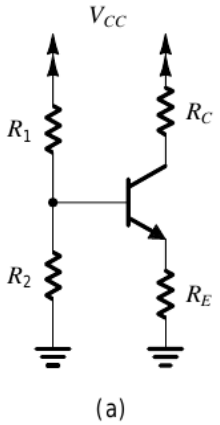
(b)

- thus Biasing by fixing V_{BE} and Biasing by fixing I_B
  - result in wide variations in I_C and V_{CE}
    - and are therefore not viable options for practical BJT amplifiers
  - the following are the practical ways of biasing a BJT, which would result in stable bias point

1. The classical discrete-circuit bias arrangement
2. A two-power-supply version of the classical bias arrangement
3. Biasing using a collector-to-base feedback resistor
4. Biasing using a constant-current source

The Classical Discrete-circuit Bias Arrangement

- An effective (and most commonly used) biasing technique for discrete BJT circuits,
  - consists of applying the base of the BJT with a fraction of the supply voltage V_{CC} through a voltage divider R_1, R_2
    - and connecting a resistance R_E in the emitter lead



(a)

- the voltage divider circuit can be replaced by its Thevenin equivalent
  - here $V_{TH} = V_{BB} = \frac{R_2}{R_2 + R_1} V_{CC}$
    - and

$$R_{TH} = R_B = R_1 \parallel R_2 = \left(\frac{1}{R_1} + \frac{1}{R_2}\right)^{-1} = \left(\frac{R_2+R_1}{R_1 R_2}\right)^{-1} = \frac{R_1 R_2}{R_1+R_2}$$

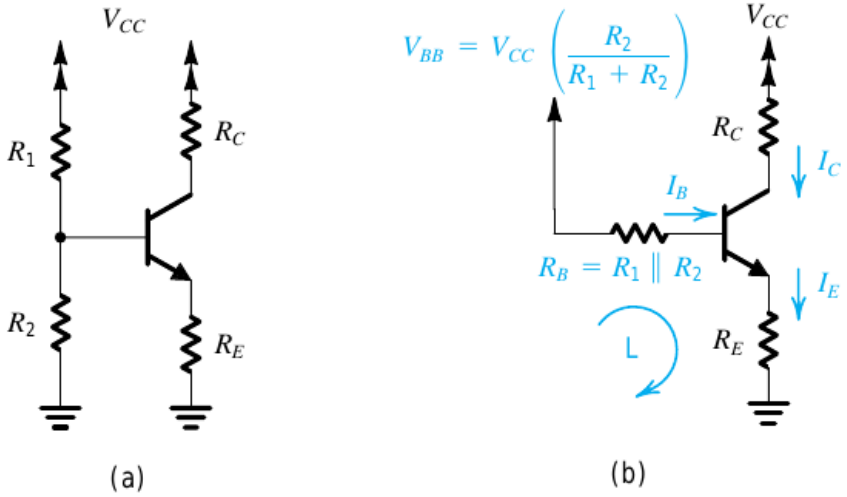
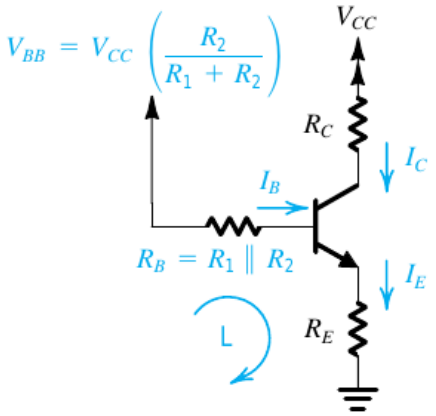


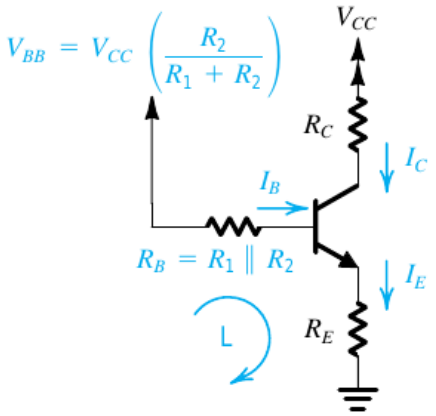
Figure 6.60 Classical biasing for BJTs using a single power supply: **(a)** circuit; **(b)** circuit with the voltage divider supplying the base replaced with its Thévenin equivalent.

- By KVL
  - $V_{BB} = I_B R_B + V_{BE} + I_E R_E$
    - As $I_B = \frac{I_E}{\beta+1}$
      - $= \Rightarrow V_{BB} = \frac{I_E}{\beta+1} R_B + V_{BE} + I_E R_E$
      - or $V_{BB} - V_{BE} = I_E\left(\frac{R_B}{\beta+1} + R_E\right)$
      - $I_E = \frac{V_{BB}-V_{BE}}{\left(\frac{R_B}{\beta+1}+R_E\right)}$
    - As $I_C = \alpha I_E$ and as α varies very little.
      - e.g. $\beta = 150 = \Rightarrow \alpha = \frac{150}{151} = 0.9934$ and $\beta = 50 = \Rightarrow \alpha = \frac{50}{51} = 0.9804$
      - $= \Rightarrow$ a stable I_E will result in equally stable I_C and vice versa



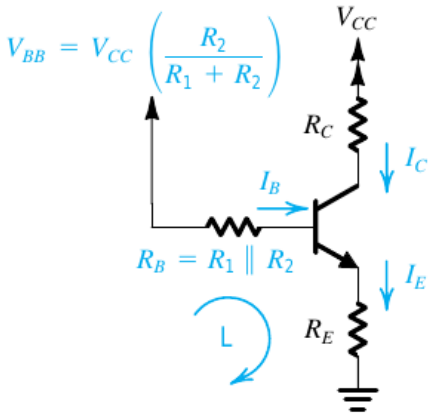
- thus $I_E = \frac{V_{BB}-V_{BE}}{\left(\frac{R_B}{\beta+1}+R_E\right)}$
  - $= \Rightarrow$ to make I_E (and hence I_C) insensitive to temperature and β variations,
    - we design the circuit to satisfy the following two constraints

1. $V_{BB} > V_{BE}$ (As V_{BE} changes with temperature)
2. and $R_E > \frac{R_B}{\beta+1}$



(b)

- Condition 1 ($V_{BB} > V_{BE}$) ensures that the numerator of the expression for I_E stays the same, despite small changes in V_{BE}
    - however there is limit, on how large V_{BB} can be made.
        - for a given value of V_{CC}, the higher the value of V_{BB}, the lower will be the sum of voltages across R_C and the V_{CB}
            - to obtain high gain and large signal swing (+ve signal swing, avoid cutoff), we need to have large value of $I_C R_C$
            - we also require large V_{CB} to ensure large signal swing (-ve signal swing, avoid saturation)
        - $I_E = \frac{V_{BB} - V_{BE}}{\left(\frac{R_B}{\beta+1} + R_E\right)}$

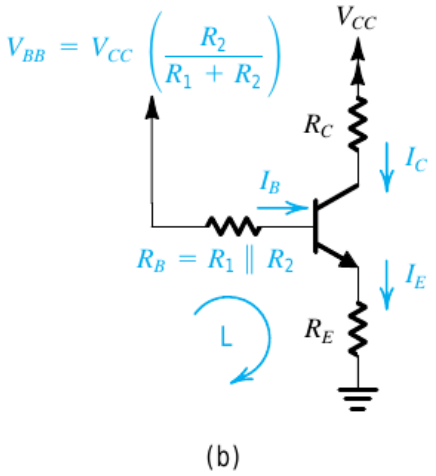


(b)

- Condition 1 ($V_{BB} > V_{BE}$)
    - thus we have a conflicting set of requirements and the solution must be a trade-off
        - As a rule of thumb, we can design for$V_{BB} \approx \frac{1}{3}V_{CC}$, $V_{CB} \approx \frac{1}{3}V_{CC}$ and $I_C R_C \approx \frac{1}{3}V_{CC}$
            - Note that here we have ignored the voltage drop across the resitor R_B
            - to include this drop, we can use $V_{BB} - I_B R_B = \frac{1}{3}V_{CC}$, $V_{CB} = \frac{1}{3}V_{CC}$ and $I_C R_C = \frac{1}{3}V_{CC}$
            - (As the KVL equation would be

$$V_{CC} = I_C R_C + V_{CB} - I_B R_B + V_{BB})$$

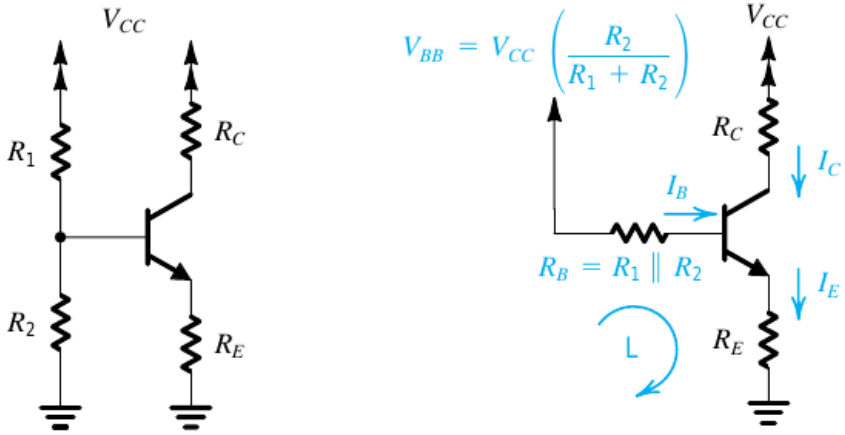
- $I_E = \frac{V_{BB} - V_{BE}}{\left(\frac{R_B}{\beta+1} + R_E\right)}$



(b)

- Also by KVL, $V_{BB} = I_B R_B + V_B = \Rightarrow V_B = V_{BB} - I_B R_B$
- thus the rule of thumb is $V_B = \frac{1}{3} V_{CC}$, $V_{CB} = \frac{1}{3} V_{CC}$ and $I_C R_C = \frac{1}{3} V_{CC}$

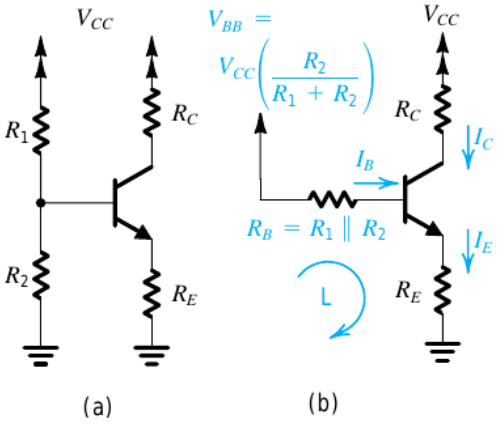
- Condition 1 ($V_{BB} > V_{BE}$)
  - thus the rule of thumb is $V_B = \frac{1}{3} V_{CC}$, $V_{CB} = \frac{1}{3} V_{CC}$ and $I_C R_C = \frac{1}{3} V_{CC}$



(a) (b)

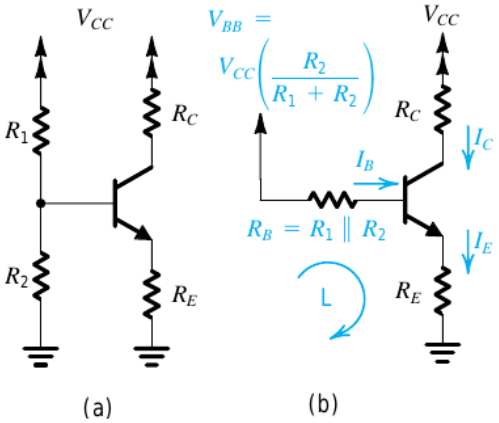
Figure 6.60 Classical biasing for BJTs using a single power supply: **(a)** circuit; **(b)** circuit with the voltage divider supplying the base replaced with its Thévenin equivalent.

- Condition 2 ($R_E > \frac{R_B}{\beta+1}$) makes I_E insensitive to variations in β
  - and could be satisfied by selecting R_B small
    - As $R_B = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2}$, R_B = small means low values for R_1 and R_2
      - $= \Rightarrow$ the input resistance of the amplifier is lowered (if the input is coupled to the base, R_1 and R_2 will appear in parallel between the base and ground)
    - $I_E = \frac{V_{BB} - V_{BE}}{\left(\frac{R_B}{\beta+1} + R_E\right)}$

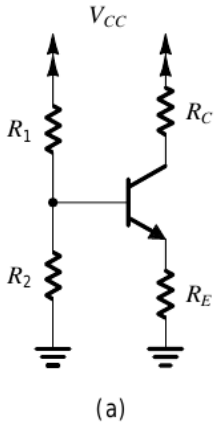


- Note that this condition($R_E > \frac{R_B}{\beta+1}$) $\Rightarrow = R_B = R_1 \parallel R_2$ is very small i.e. the base voltage is independent of the value of the β and is determined solely by the voltage divider

- Condition 2 ($R_E > \frac{R_B}{\beta+1}$)
  - this condition can be satisfied by setting the current in the divider to be much larger than the base current
    - typically one selects R_1 and R_2 such that their current is in the range of I_E to $0.1I_E$
    - $I_E = \frac{V_{BB}-V_{BE}}{\left(\frac{R_B}{\beta+1}+R_E\right)}$



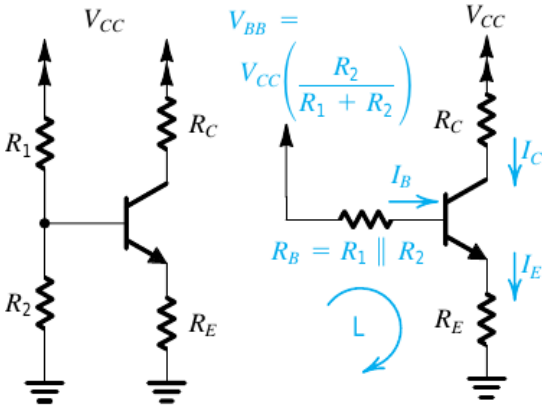
- Note that here the resistor R_E tend to stabilize the bias current I_E (and hence I_C)
  - Consider that for some reason the emitter current increases.
    - $= \Rightarrow$ the voltage drop across R_E and hence V_E will increase
    - As because of condition 2, V_B is determined primarily by voltage divider R_1, R_2 i.e. V_B will stay fixed
    - $= \Rightarrow V_{BE} = V_B - V_E$ has decreased
    - this in turn will reduce the emitter (and collector) current
    - thus R_E stabilizes the bias current



(a)

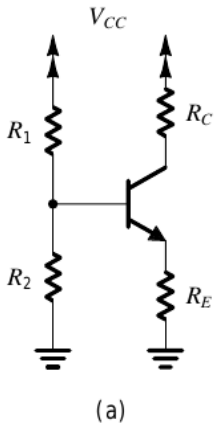
Example 6.20

- We wish to design the bias network of the amplifier in Fig. 6.60 to establish a current $I_E = 1mA$ using a power supply $V_{CC} = +12V$. The transistor is specified to have a nominal β value of 100.



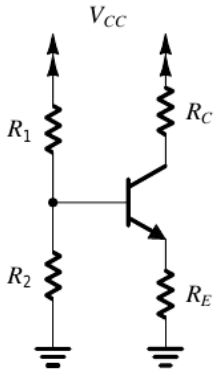
(a) (b)

- here $I_E = 1mA$, $V_{CC} = 12V$, $\beta = 100$
  - $= \Rightarrow \alpha = \frac{\beta}{\beta+1} = \frac{100}{101} = 0.9901$
    - $I_C = \alpha I_E = 0.9901 \times 1m = 0.9901mA$
    - As a rule of thumb, this biasing circuit can be designed by setting
      - $V_B = \frac{1}{3}V_{CC}$, $V_{CB} = \frac{1}{3}V_{CC}$ and $I_C R_C = \frac{1}{3}V_{CC}$
      - here last two conditions ($V_{CB} = \frac{1}{3}V_{CC}$ and $I_C R_C = \frac{1}{3}V_{CC}$) will ensure enough signal swing
      - 1st condition ($V_B = \frac{1}{3}V_{CC}$) will ensure bias point stability
    - $= \Rightarrow V_B = 4V$, $V_{CB} = 4V$ and $I_C R_C = 4V$



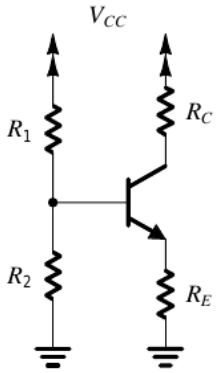
(a)

- $V_B = 4V$, $V_{CB} = 4V$ and $I_C R_C = 4V$
  - $V_{CB} = 4V = \Rightarrow V_C - V_B = 4V$ or $V_C = V_B + 4 = 8V$
    - As $V_{BE} = 0.7V = \Rightarrow V_B - V_E = 4 - V_E = 0.7$ or $V_E = 4 - 0.7 = 3.3V$
    - by ohms law
      - $I_E R_E = V_E = 3.3 = \Rightarrow R_E = \frac{V_E}{I_E} = \frac{3.3}{1m} = 3.3k\Omega$
    - As $I_C R_C = 4V$ and $I_C = 0.9901mA$
      - $= \Rightarrow R_C = \frac{4}{I_C} = \frac{4}{0.9901m} = 4.04k\Omega$
    - As the current through R_2 can be set to be in the range of I_E to $0.1I_E$



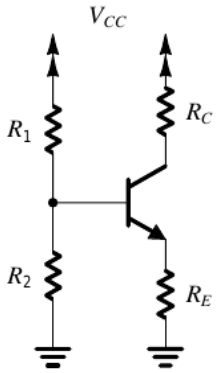
(a)

- Design 1: for $I_{R2} = 0.1I_E$
  - $I_{R2} = 0.1 \times 1m = 0.1mA$
    - by ohms law
      - $I_{R2} = \frac{V_B}{R_2} = \Rightarrow R_2 = \frac{V_B}{I_{R2}} = \frac{4}{0.1m} = 40k\Omega$
      - Also by ohms law
      - $I_{R1} = \frac{V_{CC} - V_B}{R_1} = \frac{12-4}{R_1}$ or $R_1 = \frac{8}{I_{R1}}$
      - By KCL
      - $I_{R1} = I_{R2} + I_B = 0.1m + \frac{I_E}{\beta+1} = 0.1m + \frac{1m}{101} = 0.1099mA$
      - $= \Rightarrow R_1 = \frac{8}{I_{R1}} = \frac{8}{0.1099m} = 72.793k\Omega$
      - to confirm $I_E = \frac{V_{BB} - V_{BE}}{\left(\frac{R_B}{\beta+1} + R_E\right)}$
      - here $V_{BB} = \frac{V_{CC} R_2}{R_1 + R_2} = \frac{12 \times 40k}{72.793k + 40k} = \frac{480k}{112.793k} = 4.2556V$, $R_B = R_1 \parallel R_2 = 25.815k\Omega$
      - $I_E = \frac{V_{BB} - V_{BE}}{\left(\frac{R_B}{\beta+1} + R_E\right)} = \frac{4.2556 - 0.7}{\left(\frac{25.815k}{101} + 3.3k\right)} = 1mA$



(a)

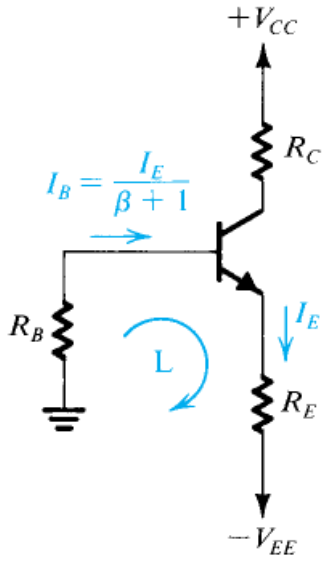
- Design 2: for $I_{R2} = I_E$
  - $I_{R2} = 1m = 1mA$
    - by ohms law
      - $I_{R2} = \frac{V_B}{R_2} = \Rightarrow R_2 = \frac{V_B}{I_{R2}} = \frac{4}{1m} = 4k\Omega$
      - Also by ohms law
      - $I_{R1} = \frac{V_{CC} - V_B}{R_1} = \frac{12-4}{R_1}$ or $R_1 = \frac{8}{I_{R1}}$
      - By KCL
      - $I_{R1} = I_{R2} + I_B = 1m + \frac{I_E}{\beta+1} = 1m + \frac{1m}{101} = 1.0099mA$
      - $= \Rightarrow R_1 = \frac{8}{I_{R1}} = \frac{8}{1.0099m} = 7.9216k\Omega$



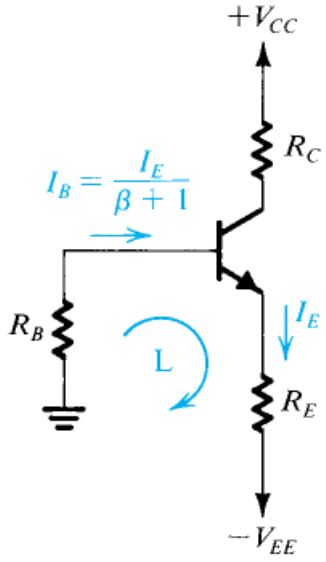
(a)

A Two-Power-Supply Version of the Classical Bias Arrangement

- if two power supplies are available, a relatively simpler biasing arrangement can be used
  - By KVL along L
    - $I_B R_B + V_{BE} + I_E R_E - V_{EE} = 0$
    - as $I_B = \frac{I_E}{\beta+1}$
      - $\frac{I_E}{\beta+1} R_B + V_{BE} + I_E R_E = V_{EE}$
      - $I_E \left(\frac{R_B}{\beta+1} + R_E \right) = V_{EE} - V_{BE}$
      - or $I_E = \frac{V_{EE} - V_{BE}}{R_E + \frac{R_B}{\beta+1}}$
    - $I_E = \frac{V_{EE} - V_{BE}}{R_E + \frac{R_B}{\beta+1}}$



- $I_E = \frac{V_{EE} - V_{BE}}{R_E + \frac{R_B}{\beta+1}}$
  - Note that this equation is identical to the one obtained for "Classical Discrete-Circuit Bias Arrangement" (i.e. $I_E = \frac{V_{BB} - V_{BE}}{R_E + \frac{R_B}{\beta+1}}$) except for V_{EE} replacing V_{BB}.
    - Thus the two constraints mentioned previously apply here as well
    - Note that if the transistor is to be used in common-base configuration, then R_B can be eliminated i.e. $R_B = 0$



Biasing Using a Collector-to-Base Feedback Resistor

- Another effective discrete-circuit biasing arrangement is possible by
  - connecting a feedback resistor R_B between the collector and the base

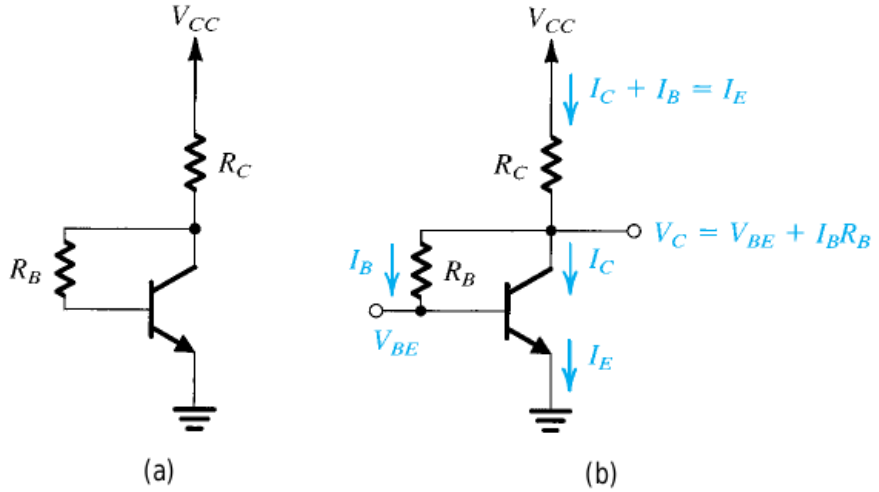
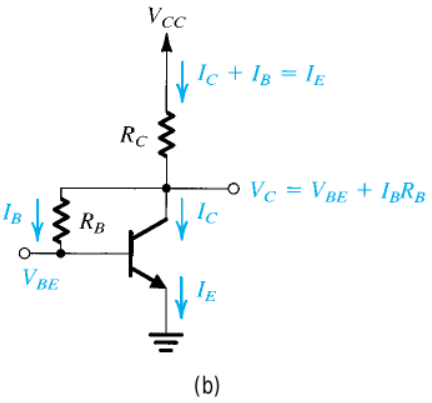


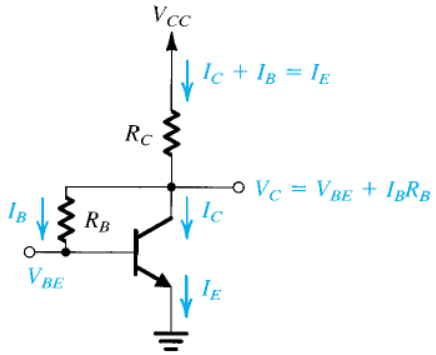
Figure 6.62 **(a)** A common-emitter transistor amplifier biased by a feedback resistor R_B. **(b)** Analysis of the circuit in **(a)**.

- by KVL, $V_{CC} = I_E R_C + I_B R_B + V_{BE}$
  - as $I_B = \frac{I_E}{\beta+1}$
    - $V_{CC} = I_E R_C + \frac{I_E}{\beta+1} R_B + V_{BE}$
      - $V_{CC} - V_{BE} = I_E R_C + \frac{I_E}{\beta+1} R_B$
      - $V_{CC} - V_{BE} = I_E \left(R_C + \frac{1}{\beta+1} R_B \right)$
      - $\frac{V_{CC} - V_{BE}}{R_C + \frac{1}{\beta+1} R_B} = I_E$
    - $I_E = \frac{V_{CC} - V_{BE}}{R_C + \frac{R_B}{\beta+1}}$



  - Note that this equation is identical to the one obtained for "Classical Discrete-Circuit Bias Arrangement" (i.e. $I_E = \frac{V_{BB} - V_{BE}}{R_E + \frac{R_B}{\beta+1}}$) except for V_{CC} replacing V_{BB}.
  - thus this circuit does provide bias point stability
- i.e. to obtain stable bias point
  - $V_{CC} > V_{BE}$
    - and $R_C > \frac{R_B}{\beta+1}$
    - Also note that in this circuit arrangement, the allowable negative signal swing at the collector is determined by the value of R_B
      - by KVL

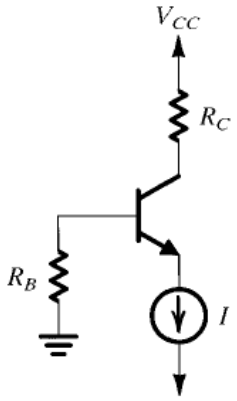
- $V_{CB} = I_B R_B = \frac{I_E R_B}{\beta+1}$



(b)

Biasing Using a Constant-Current Source

- Another effective way for biasing a BJT is shown in fig and it utilizes a constant-current source I
  - This circuit has the advantage that the emitter current is independent
    - of the values of β and R_B
    - thus R_B can be made large, enabling an increase in the input resistance at the base
      - without adversely affecting bias stability



(a)

- the current source I can be implemented by the circuit (known as current mirror) shown in fig b

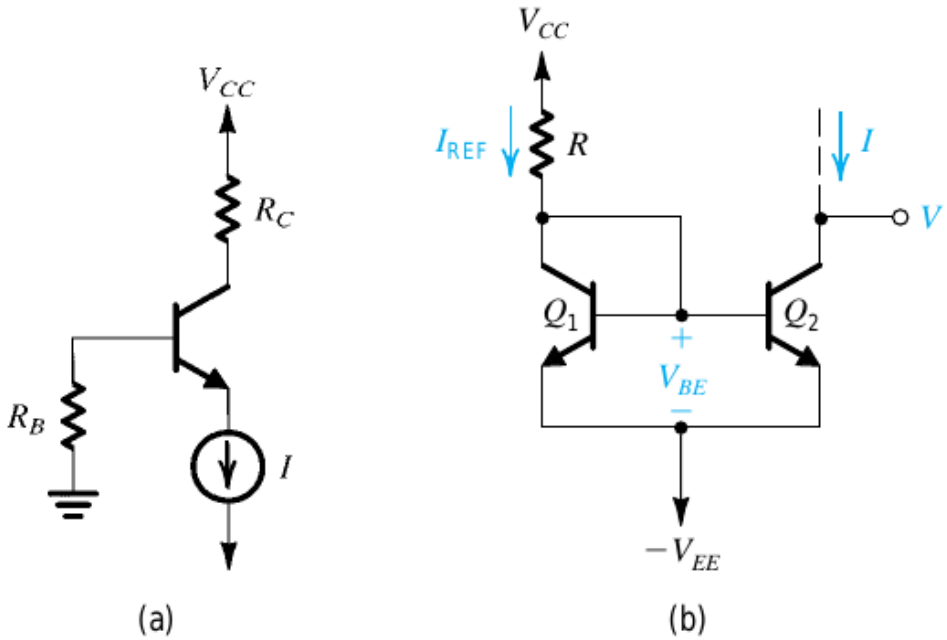
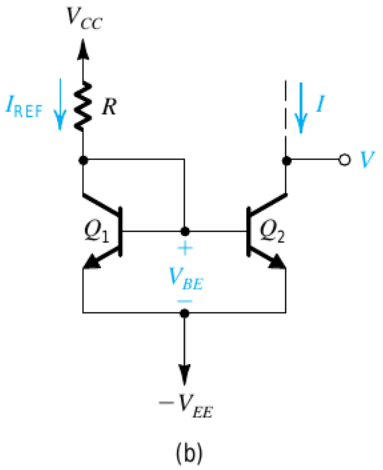


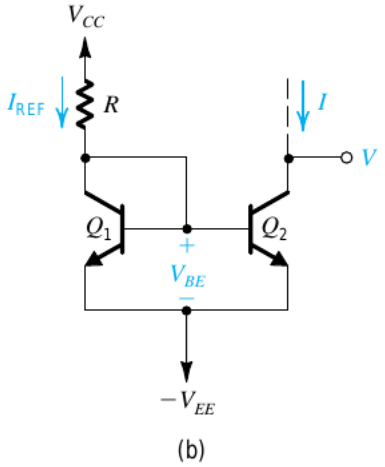
Figure 6.63 **(a)** A BJT biased using a constant-current source I. **(b)** Circuit for implementing the current source I.

- The circuit utilizes a pair of matched transistors Q_1 and Q_2
  - the transistor Q_1 is connected as a diode by shorting its collector to its base
    - By KVL
      - $V_{CC} = I_{REF}R + V_{BE} + (-V_{EE})$
      - $V_{CC} = I_{REF}R + V_{BE} - V_{EE}$
      - $I_{REF} = \frac{V_{CC}+V_{EE}-V_{BE}}{R}$
    - Assuming that Q_1 and Q_2have high β values,
      - we can neglect their base currents
      - $= \Rightarrow I_{REF} = I_{C,Q1}$



- As Q_1 and Q_2 have the same V_{BE}
  - $= \Rightarrow$their collector currents will be equal
    - $= \Rightarrow I_{C,Q2} = I_{C,Q1} = I = I_{REF}$
    - thus $I = I_{REF} = \frac{V_{CC}+V_{EE}-V_{BE}}{R}$
    - Neglecting the Early Effect in Q_2,
      - the collector current $I = I_{C,Q2}$ will remain constant at this value $\left(\frac{V_{CC}+V_{EE}-V_{BE}}{R}\right)$

- as long as the transistor Q_2 stays in active region.
- i.e. as long as the voltage at the collector is kept greater than that at the emitter by at least 0.3V $(V_{CE} \geq 0.3)$



(b)

Exercise 6.47

Exercise D6.48

Exercise D6.49

Exercise 6.50
