Lecture 5a

EE-215 Electronic Devices and Circuits

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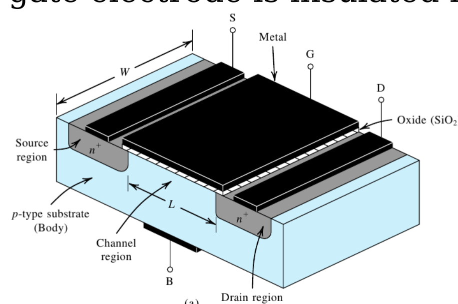
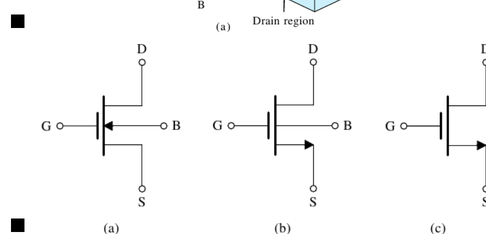
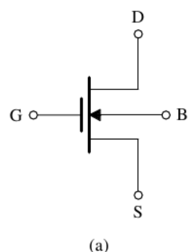
Current-Voltage Characteristics

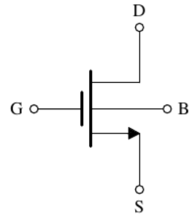
Circuit Symbol

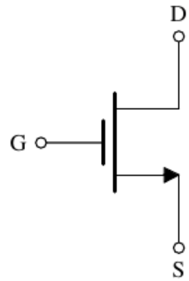
- the circuit symbols for an n-channel enhancement type MOSFET are shown here
    - the two vertical lines represent the gate and the channel
        - the spacing between the two lines indicate that the gate electrode is insulated from the substrate
        - 

        - 

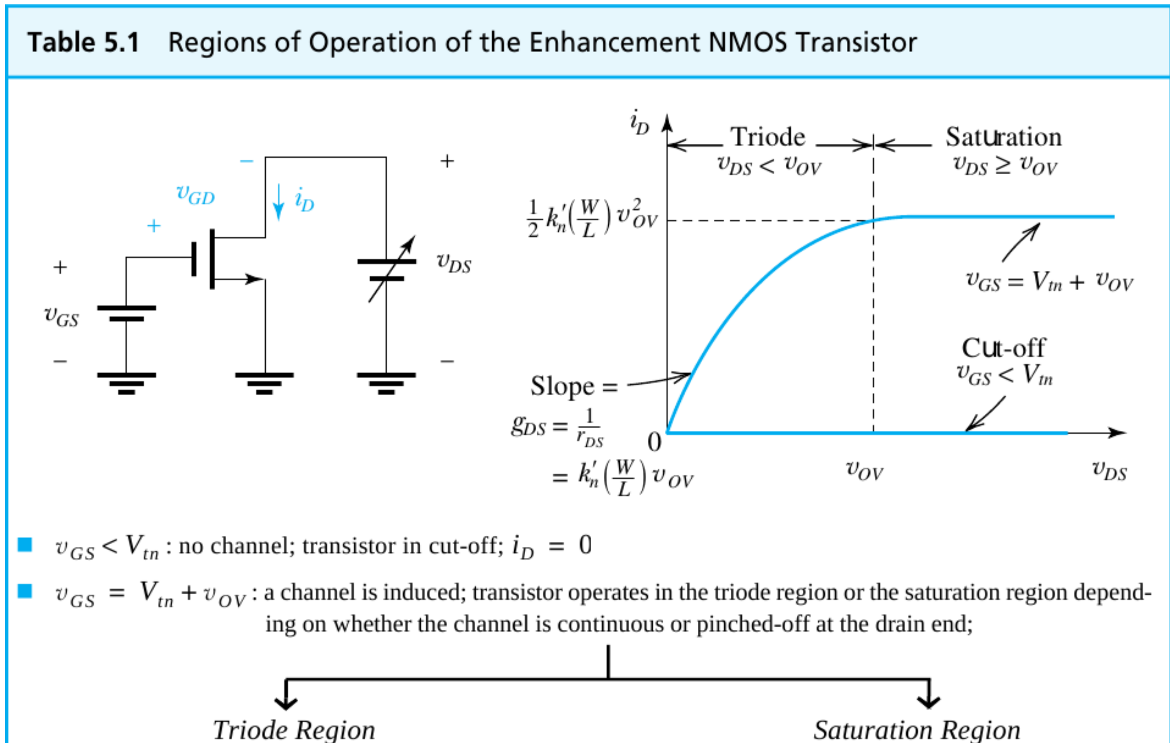
- the arrow indicates the polarity of the substrate (p-type) and the channel (n-type)
    - the arrow points from the p-type substrate to the n-type channel
        - thus the arrow indicates that this is an n-channel MOSFET
        - 

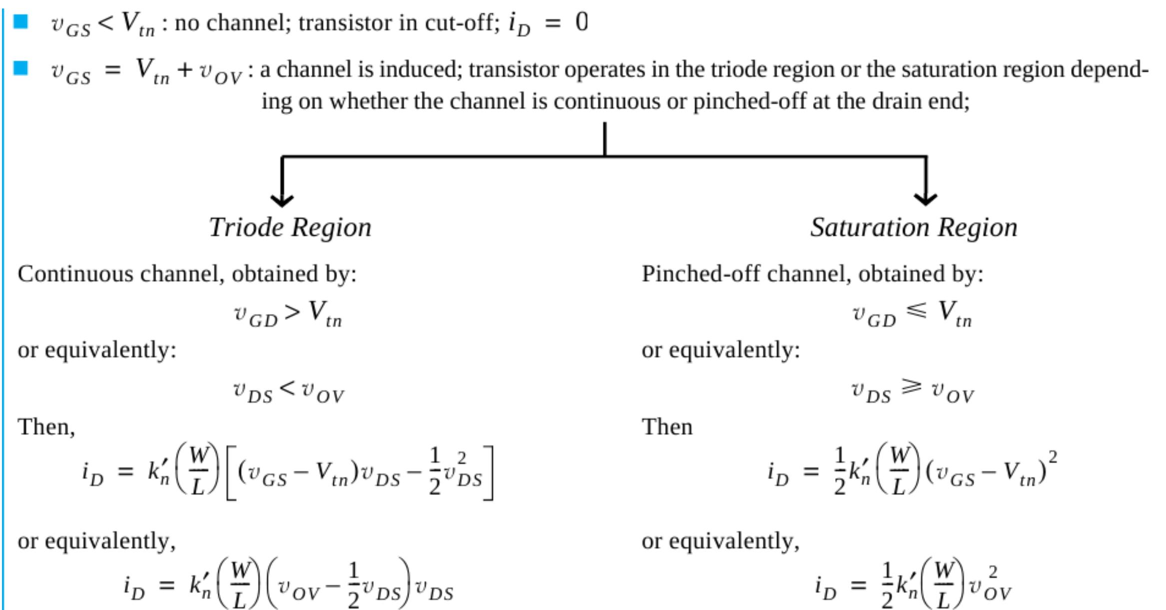
- when it is required to designate one terminal as the source and the other as the drain, this symbol is more convenient
    - here the arrow head is placed at the source terminal
        - and the arrowhead points in the direction of current flow
        - recall that for an n-channel MOSFET, electrons flow from the source to the drain

- $= \Rightarrow$ current flows from the drain to the source
- 

- when the source is connected to the body of the device,
  - a simplified circuit symbol can be used
    - 

The $i_D - v_{DS}$ Characteristics

- for an NMOS transistor, there are three possible regions of operation
  - the cutoff region
  - the triode region
  - the saturation region
- 

- 

  - $v_{GS} < V_{tn}$: no channel; transistor in cut-off; $i_D = 0$
  - $v_{GS} = V_{tn} + v_{OV}$: a channel is induced; transistor operates in the triode region or the saturation region depending on whether the channel is continuous or pinched-off at the drain end;

  Triode Region

  Continuous channel, obtained by:

  $$v_{GD} > V_{tn}$$

  or equivalently:

  $$v_{DS} < v_{OV}$$

  Then,

  $$i_D = k_n'\left(\frac{W}{L}\right)\left[(v_{GS} - V_{tn})v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

  or equivalently,

  $$i_D = k_n'\left(\frac{W}{L}\right)\left(v_{OV} - \frac{1}{2}v_{DS}\right)v_{DS}$$

  Saturation Region

  Pinched-off channel, obtained by:

  $$v_{GD} \leqslant V_{tn}$$

  or equivalently:

  $$v_{DS} \geqslant v_{OV}$$

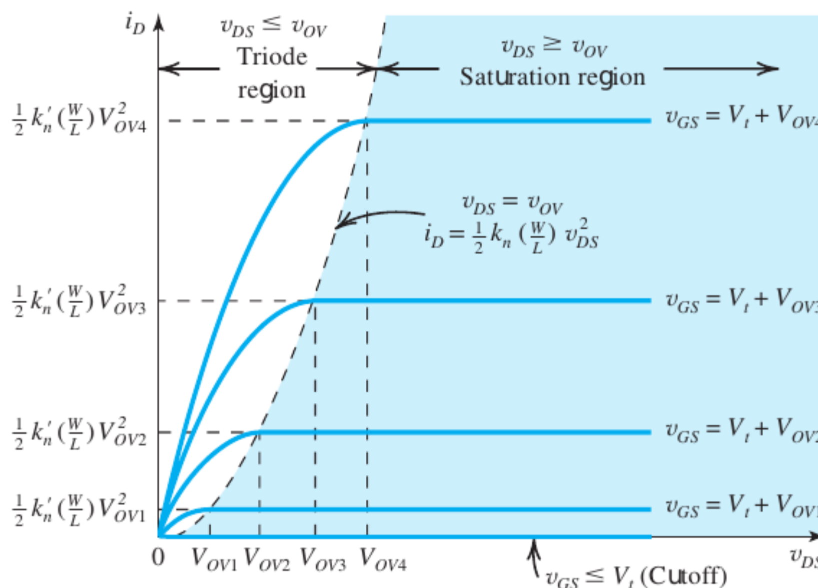
  Then

  $$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2$$

  or equivalently,

  $$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)v_{OV}^2$$

- $i_D - v_{DS}$ characteristic for the NMOS transistor with different v_{GS} settings is shown in fig



  - **Figure 5.13** The i_D–v_{DS} characteristics for an enhancement-type NMOS transistor.

- Note that the boundary between the triode and the saturation regions, can be given as
  - $i_D = \frac{1}{2}k_n'(\frac{W}{L})v_{DS}^2$
    - $\because i_D = \frac{1}{2}k_n'(\frac{W}{L})v_{OV}^2$ and
    - $v_{OV} = v_{DS}$ at the start of saturation region

The $i_D - v_{GS}$ Characteristics

- A MOSFET operating in the saturation region, can be used to design an amplifier
  - in saturation, the drain current is a constant (i.e. doesnot change whith v_{DS})
    - and is determined by v_{GS} (or v_{OV}) and is independent of v_{DS}

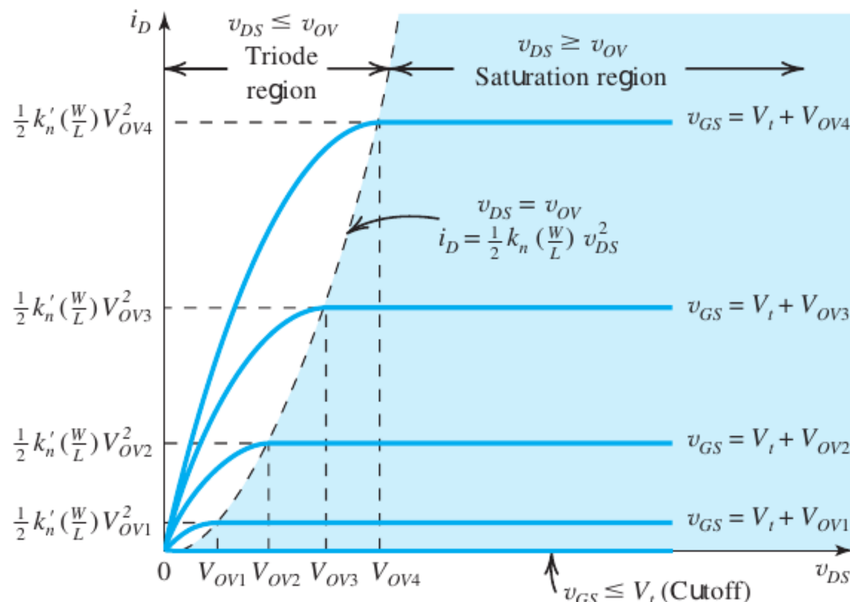
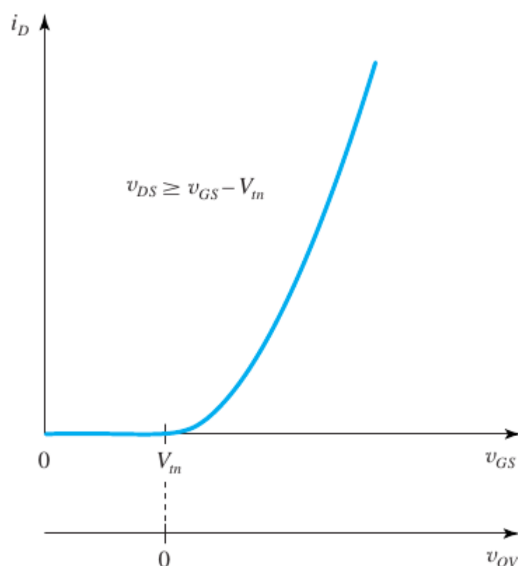


Figure 5.13 The i_D–v_{DS} characteristics for an enhancement-type NMOS transistor.

- $= \Rightarrow$ the MOSFET operates as a constant-current source, whose current is determined by v_{GS}(or v_{OV})
- thus the MOSFET is a voltage controlled current source with the control relationship given as
- $i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2$ or $i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)v_{OV}^2$

- the $i_D - v_{GS}$ characteristics of an NMOS transistor operating in saturation region can be given as
  - 

  - thus the MOSFET in the saturation region acts as a voltage-controlled current source
- the MOSFET in the saturation region acts as
  - a voltage-controlled current source and can be modeled as

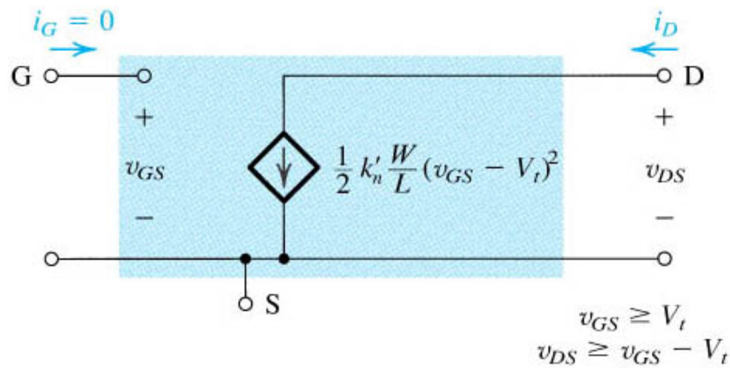


Figure 4.13 Large-signal equivalent-circuit model of an *n*-channel MOSFET operating in the saturation region.

- this equivalent circuit is known as large signal equivalent circuit model
- Note that the current source is ideal i.e. it has an infinite output resistance
- $= \Rightarrow$ which represents that i_D is independent of v_{DS} in saturation region.
- In practice, this output resistance is finite because of channel-length modulation.

Finite Output Resistance in Saturation

- Uptill now, we have assumed that in saturation, i_D is independent of v_{DS}
  - $i_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right) (v_{GS} - V_{tn})^2$

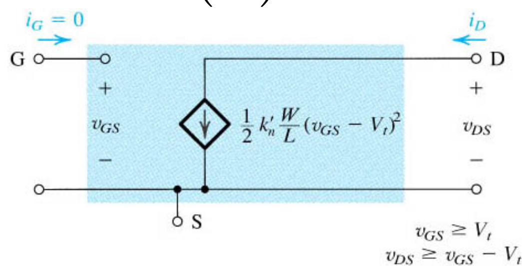


Figure 4.13 Large-signal equivalent-circuit model of an *n*-channel MOSFET operating in the saturation region.

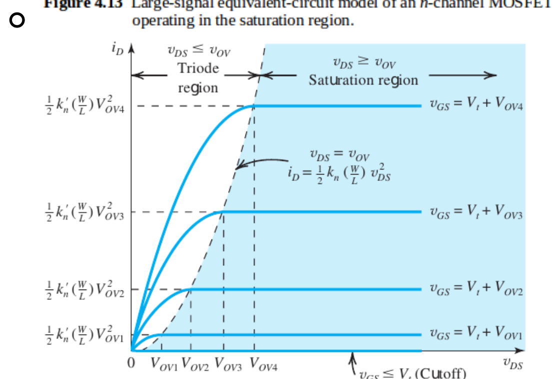
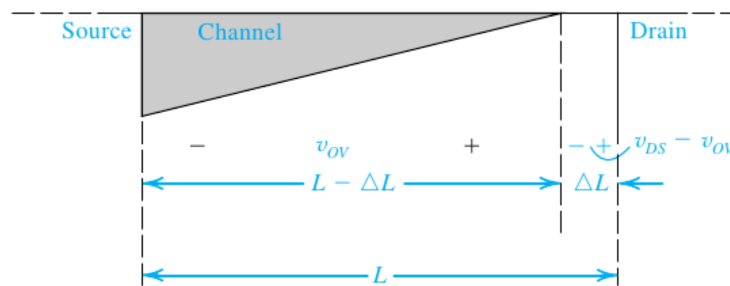


Figure 5.13 The i_D–v_{DS} characteristics for an enhancement-type NMOS transistor.

  - i.e. a change Δv_{DS} in the drain to source voltage causes a zero change in i_D
  - $= \Rightarrow$ that the incremental resistance looking into the drain of a saturated MOSFET is infinite
- this is not true in practice

- As v_{DS} is increased, the channel pinch-off point is
  - moved slightly avay from the drain, towards the source.



- **Figure 5.16** Increasing v_{DS} beyond v_{DSsat} causes the channel pinch-off point to move slightly away from the drain, thus reducing the effective channel length (by ΔL).
- Note that the voltage across the channel still remains constant at v_{OV}
- Note that the voltage across the channel still remains constant at v_{OV},
  - while the additional voltage applied to the drain appears as a voltage across
  - the depletion region between the end of the channel and the drain
- so the channel length is now reduced from L to $L - \Delta L$
- and this phenomenon is called channel-length modulation

- As i_D is inversely proportional to the channel length
  - $i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2$ for $v_{DS} = v_{OV}$
  - $= \Rightarrow i_D$ increases with v_{DS} as L decreases with v_{DS} because of channel-length modulation
  - To account for the dependance of i_D on v_{DS} in saturation,
    - we replace L in the above equation by $L - \Delta L$
  - $= \Rightarrow i_D = \frac{1}{2}k_n'\left(\frac{W}{L - \Delta L}\right)(v_{GS} - V_{tn})^2$
    - multiply and divide by L
    - $i_D = \frac{1}{2}k_n'\frac{W}{L}\left(\frac{L}{L - \Delta L}\right)(v_{GS} - V_{tn})^2$
    - $i_D = \frac{1}{2}k_n'\frac{W}{L}\left(\frac{L - \Delta L}{L}\right)^{-1}(v_{GS} - V_{tn})^2$
    - $i_D = \frac{1}{2}k_n'\frac{W}{L}\left(1 - \frac{\Delta L}{L}\right)^{-1}(v_{GS} - V_{tn})^2$
  - $i_D = \frac{1}{2}k_n'\frac{W}{L}(v_{GS} - V_{tn})^2\left(1 - \frac{\Delta L}{L}\right)^{-1}$
- $i_D = \frac{1}{2}k_n'\frac{W}{L}(v_{GS} - V_{tn})^2\left(1 - \frac{\Delta L}{L}\right)^{-1}$
  - assuming $\Delta L < L = \Rightarrow \frac{\Delta L}{L} < 1$
    - As for $|x| < 1$, $(1 \pm x)^n \approx 1 \pm nx$
    - $= \Rightarrow \left(1 - \frac{\Delta L}{L}\right)^{-1} \approx 1 - \left(-1\right)\frac{\Delta L}{L} = 1 + \frac{\Delta L}{L}$

- $i_D = \frac{1}{2} k_n' \frac{W}{L} (v_{GS} - V_{tn})^2 \left(1 + \frac{\Delta L}{L}\right)$
- as ΔL increases by increasing $v_{DS} \implies \Delta L \propto v_{DS}$
  - let the proportionality constant be λ'
  - $\implies \Delta L = \lambda' v_{DS}$ and $\frac{\Delta L}{L} = \frac{\lambda' v_{DS}}{L} = \lambda v_{DS}$
- $\implies i_D = \frac{1}{2} k_n' \frac{W}{L} (v_{GS} - V_{tn})^2 \left(1 + \lambda v_{DS}\right)$
- where λ is a device parameter having the units of V^{-1}
- the value of λ depends on the process technology and on the channel length L

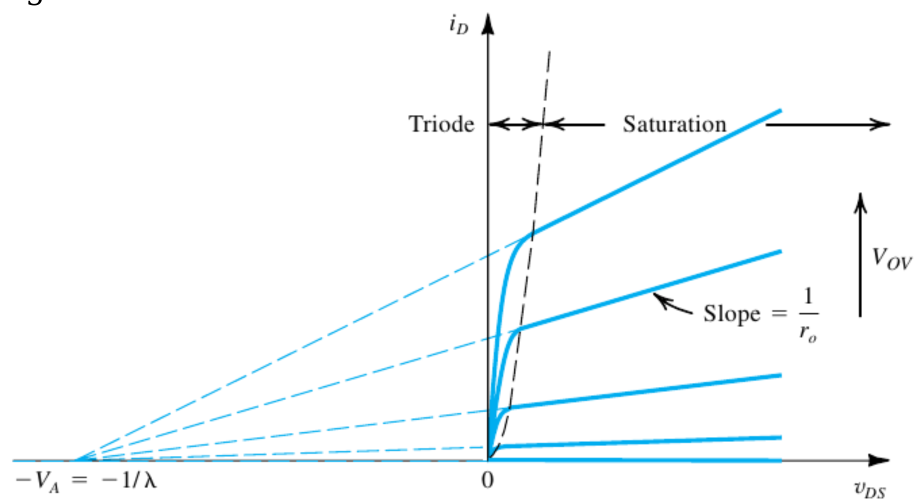
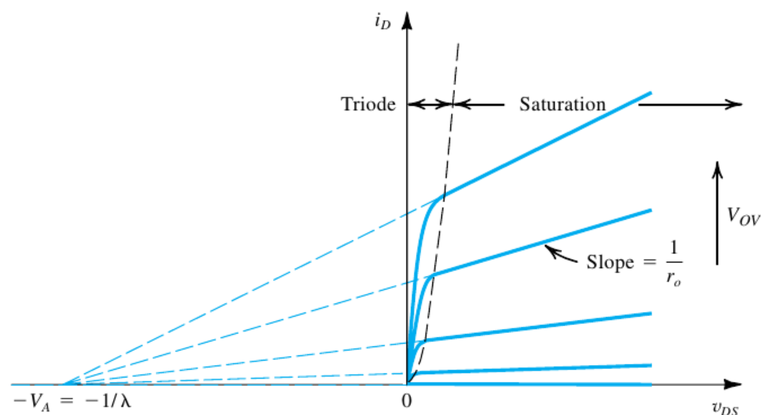
- because of this channel-length modulation,
  - there is a linear dependence of i_D on v_{DS} in the saturation region
  - 

    Figure 5.17 Effect of v_{DS} on i_D in the saturation region. The MOSFET parameter V_A depends on the process technology and, for a given process, is proportional to the channel length L.

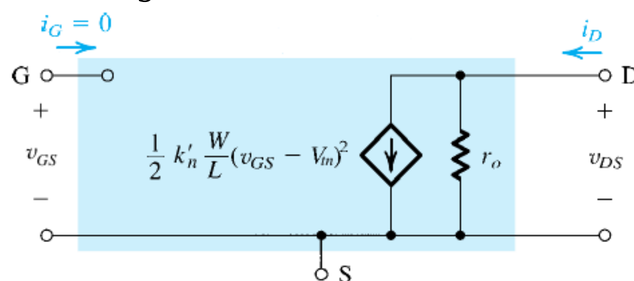
- if these straight lines are extrapolated,
  - they all intersect the v_{DS} axis at the same point $v_{DS} = -V_A$,
    - where V_A is a positive voltage called Early voltage,$V_A = \frac{1}{\lambda}$
  - V_A is a device parameter. its value is dependent on the process and the channel length.
    - i.e. $V_A = V_A' L$ where V_A' is entirely process technology dependent

- thus becuase of the channel length modualation
  - value of i_D depends on v_{DS} , in the saturation region
  - so for a given v_{GS}, a change Δv_{DS}
    - $\implies$ corresponding change Δi_D in the drain current i_D



- **Figure 5.17** Effect of v_{DS} on i_D in the saturation region. The MOSFET parameter V_A depends on the process technology and, for a given process, is proportional to the channel length L.

- $= \Rightarrow$ the output resistance of the current source representing i_D in saturation
  - is no longer infinite. but is a finite value represented by r_o

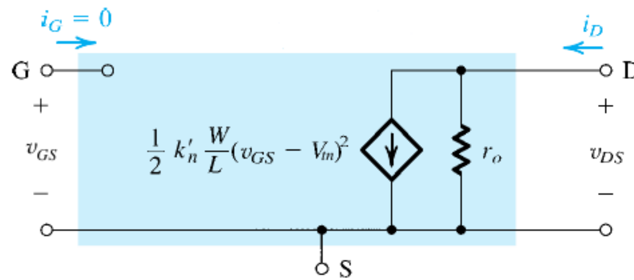


  - **Figure 5.18** Large-signal equivalent circuit model of the n-channel MOSFET in saturation, incorporating the output resistance r_o. The output resistance models the linear dependence of i_D on v_{DS} and is given by Eq. (5.23).
  - where $r_o = \left[\frac{\partial i_D}{\partial v_{DS}}\right]^{-1}_{v_{GS}=constant}$

- $r_o = \left[\frac{\partial i_D}{\partial v_{DS}}\right]^{-1}_{v_{GS}\ constant}$
  - $r_o = \left[\frac{\partial}{\partial v_{DS}}\left\{\frac{1}{2}k_n{'}\frac{W}{L}(v_{GS}-V_{tn})^2\left(1+\lambda v_{DS}\right)\right\}\right]^{-1}_{v_{GS}\ constant}$
  - $r_o = \left[\frac{1}{2}k_n{'}\frac{W}{L}(v_{GS}-V_{tn})^2\frac{\partial}{\partial v_{DS}}\left(1+\lambda v_{DS}\right)\right]^{-1}$
  - $r_o = \left[\frac{1}{2}k_n{'}\frac{W}{L}(v_{GS}-V_{tn})^2\left(0+\lambda(1)\right)\right]^{-1}$
  - $r_o = \left[\frac{1}{2}k_n{'}\frac{W}{L}(v_{GS}-V_{tn})^2\lambda\right]^{-1}$
  - $r_o = \frac{1}{\lambda}\left[\frac{1}{2}k_n{'}\frac{W}{L}(v_{GS}-V_{tn})^2\right]^{-1} = \frac{1}{\lambda}[I_D]^{-1}$
  - $r_o = \frac{1}{\lambda I_D} = \frac{V_A}{I_D}$
  - where I_D is the drain current without channel-length modulation effect i.e. $I_D = \frac{1}{2}k_n{'}\frac{W}{L}(v_{GS}-V_{tn})^2$

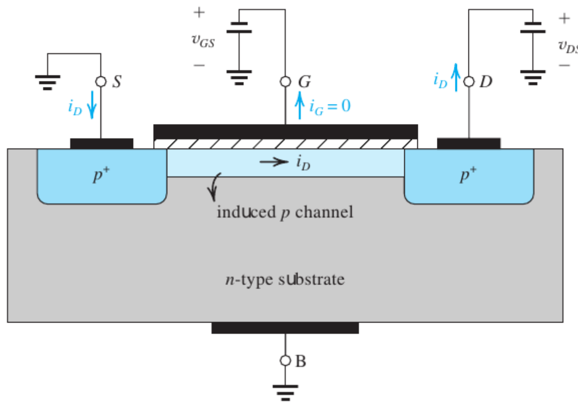
- $r_o = \frac{1}{\lambda I_D} = \frac{V_A}{I_D}$

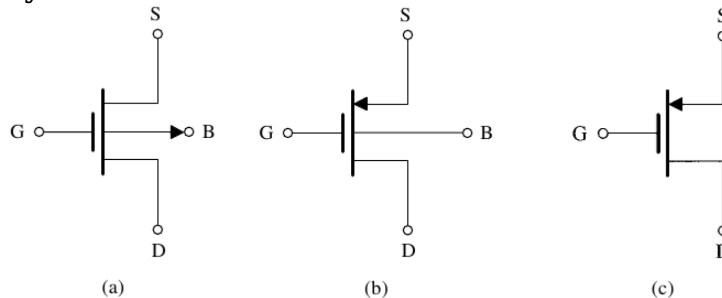
- $\implies r_o \propto \frac{1}{I_D}$
- thus the large-signal equivalent circuit model incorporating the channel-length modulation i.e. r_o can be given as

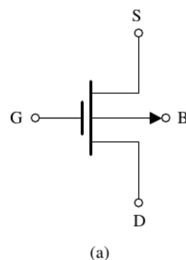


- **Figure 5.18** Large-signal equivalent circuit model of the n-channel MOSFET in saturation, incorporating the output resistance r_o. The output resistance models the linear dependence of i_D on v_{DS} and is given by Eq. (5.23).

Characteristics of the p-Channel MOSFET

- 

    - the p-channel enhancement type MOSFET, has the circuit symbol of
    - 

- the arrow indicates that the channel is p-type (tail of arrow)
    - while the substrate is n-type (head of arrow)
        - 

- this symbol is utilized when it is required to designate the source terminal

- the arrow head is at the source and its direction indicates the direction of current flow
    - Note that in a p-channel MOSFET holes flow from source to the drain
    - $= \Rightarrow$ current flows from source to drain
    - (b)

- for the case where the source is connected to the substrate,
    - this simplified symbol is used
        - (c)

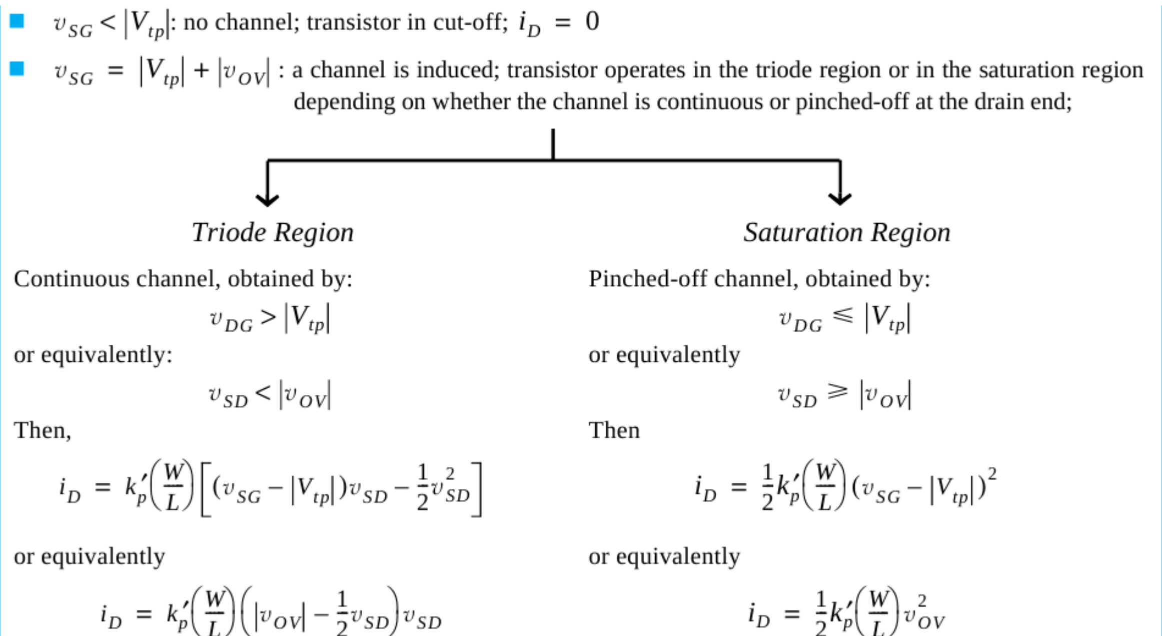
Current-Voltage Characteristics

- the regions of operation of the PMOS transistor are

Table 5.2 Regions of Operation of the Enhancement PMOS Transistor

- $v_{SG} < |V_{tp}|$: no channel; transistor in cut-off; $i_D = 0$
- $v_{SG} = |V_{tp}| + |v_{OV}|$: a channel is induced; transistor operates in the triode region or in the saturation region depending on whether the channel is continuous or pinched-off at the drain end;

Triode Region *Saturation Region*



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Triode Region

Continuous channel, obtained by:

$$v_{DG} > |V_{tp}|$$

or equivalently:

$$v_{SD} < |v_{OV}|$$

Then,

$$i_D = k_p'\left(\frac{W}{L}\right)\left[(v_{SG} - |V_{tp}|)v_{SD} - \frac{1}{2}v_{SD}^2\right]$$

or equivalently

$$i_D = k_p'\left(\frac{W}{L}\right)\left(|v_{OV}| - \frac{1}{2}v_{SD}\right)v_{SD}$$

Saturation Region

Pinched-off channel, obtained by:

$$v_{DG} \leqslant |V_{tp}|$$

or equivalently

$$v_{SD} \geqslant |v_{OV}|$$

Then

$$i_D = \frac{1}{2}k_p'\left(\frac{W}{L}\right)(v_{SG} - |V_{tp}|)^2$$

or equivalently

$$i_D = \frac{1}{2}k_p'\left(\frac{W}{L}\right)v_{OV}^2$$

- just like the NMOS transistor, the PMOS device also suffers from Channel-length modulation effect.
  - thus the saturation region expression for i_D can be given as
    - $i_D = \frac{1}{2}k_p'\left(\frac{W}{L}\right)(v_{SG} - |V_{tp}|)^2\left(1 + |\lambda| v_{SD}\right)$
    - and $\lambda = \frac{1}{V_A}$
    - where λ and V_A for the PMOS transistor are negative quantities
  - Note that for a given CMOS fabrication process, in general
    - $\lambda_n \diagdown = |\lambda_p|$ and $V_{An} \diagdown = |V_{Ap}|$