Lecture 5b

EE-215 Electronic Devices and Circuits

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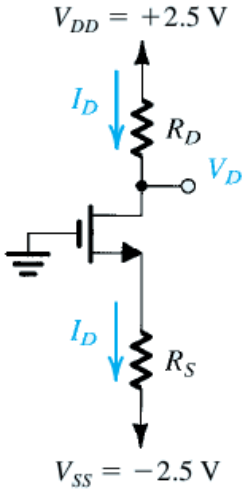
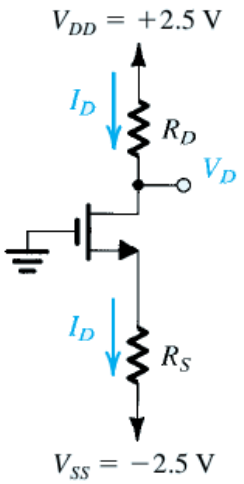
MOSFET Circuits at DC

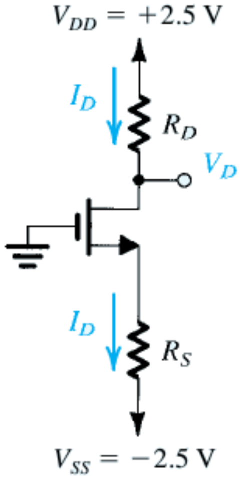
Example 5.3

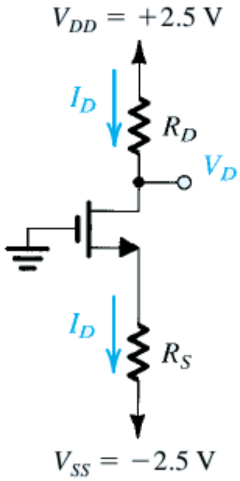
- Design the circuit of Fig. 5.21, that is, determine the values of R_D and R_S, so that the transistor operates at I_D = 0.4 mA and V_D = +0.5 V. The NMOS transistor has V_t = 0.7 V, $\mu_n C_{ox}$ = 100 μA/V^2, $L = 1\mu m$, and $W = 32\mu m$. Neglect the channel-length modulation effect (i.e., assume that $\lambda = 0$).
  - 

Solution: Example 5.3

- here
  - $R_D =?$, $R_S =?$
    - $I_D = 0.4mA$, $V_D = 0.5V$,
    - $V_t = 0.7V$, $\mu_n C_{ox} = 100\mu A/V^2$, $L = 1\mu m$, $W = 32\mu m$, $\lambda = 0$
    - As $V_D = 0.5V$, $I_D = 0.4mA$
    - Ohm's law $= \Rightarrow R_D = \frac{V_{DD}-V_D}{I_D} = \frac{2.5-0.5}{0.4m} = 5k\Omega$
    - As $I_D \searrow = 0 = \Rightarrow$ the MOSFET is on
    - so the MOSFET can be in triode region or in saturation region
    - 

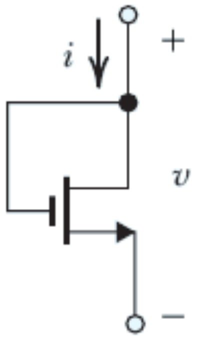
- so the MOSFET can be in triode region or in saturation region
  - As for triode region $v_{DS} < v_{OV} = v_{GS} - V_t$

- and for saturation region $v_{DS} \geq v_{OV} = v_{GS} - V_t$
  - or $v_D \geq (v_G - V_t)$
- here $v_D = 0.5$, $v_G = 0$, $V_t = 0.7 = \Rightarrow v_G - V_t = 0 - 0.7$
- $= \Rightarrow 0.5 \geq -0.7$ thus the MOSFET is in saturation region
- $i_D = \frac{1}{2} k_n\text{'} \left(\frac{W}{L}\right) v_{OV}^2 = \frac{1}{2} 100\mu \left(\frac{32}{1}\right) v_{OV}^2$
- $i_D = 0.4m = \frac{1}{2} 100\mu \left(\frac{32}{1}\right) v_{OV}^2$
- $v_{OV}^2 = \frac{0.4m}{\frac{1}{2} 100\mu \left(\frac{32}{1}\right)} = 0.25$
- 

- $v_{OV} = \sqrt{0.25} = 0.5V$
  - $v_{OV} = v_{GS} - V_t = 0.5V = \Rightarrow v_{GS} = V_t + 0.5 = 0.7 + 0.5 = 1.2V$
    - $v_G - v_S = 1.2V$
    - $0 - v_S = 1.2V$
    - $v_S = -1.2V$
    - by ohms' law
    - $R_s = \frac{v_S - V_{SS}}{I_D} = \frac{-1.2-(-2.5)}{0.4m} = \frac{-1.2+2.5}{0.4m} = 3.25k\Omega$
    - 

Example 5.4

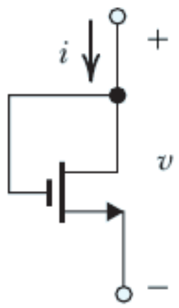
- Figure 5.22 shows an NMOS transistor with its drain and gate terminals connected together. Find the i – v relationship of the resulting two-terminal device in terms of the MOSFET parameters $k_n = k_n\text{'}(W / L)$ and V_{tn}. Neglect channel-length modulation (i.e., $\lambda = 0$) . Note that this two-terminal device is known as a diode-connected transistor.



- Figure 5.22

Solution: Example 5.4

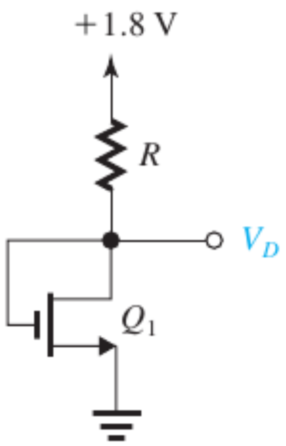
- here $v_G = v_D$
  - as for saturation region
    - $v_{DS} \geq v_{GS} - V_t$
      - $v_D \geq v_G - V_t$
      - $v_D - v_G \geq -V_t$
      - $0 \geq -V_t$ which is true for an n-channel MOSFET (as V_t is +ve value)
    - $= \Rightarrow$the MOSFET is in saturation
    - i.e. $i_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2$
    - from figure for $i = i_D$ and for $v = v_{GS}$
    - $i = \frac{1}{2} k_n' \left(\frac{W}{L}\right)(v - V_{tn})^2 = \frac{1}{2} k_n \left(v - V_{tn}\right)$



    - Figure 5.22

Exercise D5.9

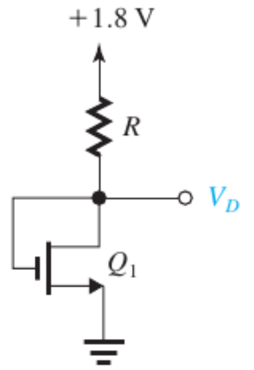
- For the circuit in Fig. E5.9, find the value of R that results in $V_D = 0.8V$. The MOSFET has $V_{tn} = 0.5V$ $\mu_n C_{ox} = 0.4mA/V^2$, $\frac{W}{L} = \frac{0.72\mu m}{0.18\mu m}$ and $\lambda = 0$



  - Figure E5.9

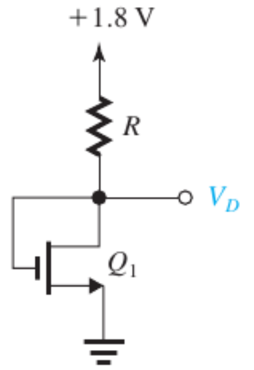
Solution: Exercise D5.9

- here
  - $V_D = 0.8V$
    - $V_{tn} = 0.5V$, $\mu_n C_{ox} = 0.4mA/V^2$, $\frac{W}{L} = \frac{0.72\mu m}{0.18\mu m}$ and $\lambda = 0$
    - from the figure $v_G = v_D$
      - $v_{DS} \geq v_{GS} - V_t$ for saturation region
      - $v_D \geq v_G - V_t$
      - $v_D - v_G \geq -V_t$
      - $v_G - v_D \leq V_t$
      - $0 \leq V_t$ which is true
      - $= \Rightarrow$the MOSFET is in saturation



    - Figure E5.9

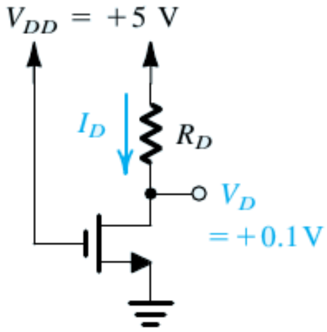
- As $v_S = 0$
  - $= \Rightarrow v_{GS} = v_G - v_S = 0.8 - 0 = 0.8V \because v_G = v_D = 0.8V$
    - $i_D = \frac{1}{2} k_n ' \left(\frac{W}{L}\right) (v_{GS} - V_{tn})^2$
      - $i_D = \frac{1}{2} 0.4m \left(\frac{0.72}{0.18}\right) (0.8 - 0.5)^2 = 72\mu A$
    - $R = \frac{1.8 - V_D}{I_D} = \frac{1.8 - 0.8}{I_D} = \frac{1}{72\mu} = 13.889k\Omega$



    - Figure E5.9

Example 5.5

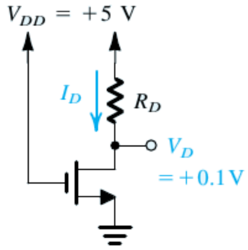
- Design the circuit in Fig. 5.23 to establish a drain voltage of $0.1V$. What is the effective resistance between drain and source at this operating point? Let $V_{tn} = 1V$ and $k_n '(W/L) = 1mA/V^2$.



- Figure 5.23

Solution: Example 5.5

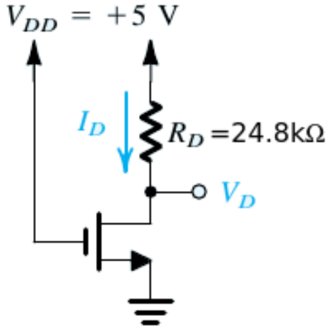
- here $v_{GS} = v_G - v_S = V_{DD} - 0 = 5 - 0 = 5V$
  - $v_{DS} = v_D - v_S = 0.1 - 0 = 0.1V$
    - $= \Rightarrow v_{DS} < v_{GS} - V_t$
      - $0.1 < 5 - 1$
      - $0.1 < 4 = \Rightarrow$ triode region
    - for triode region
      - $i_D = k_n'\left(\frac{W}{L}\right)\left[\left(v_{GS} - V_{tn}\right)v_{DS} - \frac{1}{2}v_{DS}^2\right]$
      - $i_D = 1m\left[\left(5 - 1\right)0.1 - \frac{1}{2}(0.1)^2\right]$
      - $i_D = 1m[0.4 - 0.005] = 0.395mA$
    - $r_{DS} = \frac{v_{DS}}{i_D} = \frac{0.1}{0.395m} = 253.16\Omega$
    - $R_D = \frac{V_{DD} - v_D}{i_D} = \frac{5 - 0.1}{0.395m} = 12.405k\Omega$



- Figure 5.23

Exercise 5.11

- If in the circuit of Example 5.5 the value of R_D is doubled, find approximate values for I_D and V_D.

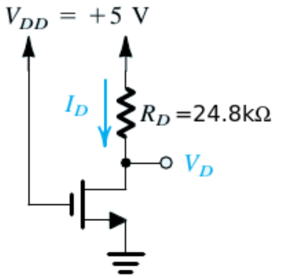


- Figure for Exercise 5.11

Exercise 5.11: (Exact Analysis)

- Now R_D is doubled
  - $= \Rightarrow R_D = 2 \times 12.4k\Omega = 24.8k\Omega$

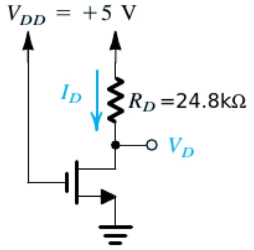
- As $V_{GS} > V_t$ i.e. $5 > 1 = \Rightarrow$mosfet is not cutoff
- Assume Saturation mode
  - $I_D = \frac{1}{2}k_n\text{'}\frac{W}{L}(V_{GS} - V_t)^2 = \frac{1}{2}\left(1m\right)(4)^2 = \frac{16m}{2} = 8mA$
  - ohms law $= \Rightarrow V_{DD} - V_D = I_D R_D$
    - $5 - V_D = (8m)(24.8k)$
    - $5 - V_D = 198.4$
    - $= \Rightarrow 5 - 198.4 = V_D$
    - or $V_D = -193.4V$
    - Now for saturation$V_{DS} \geq V_{GS} - V_t = \Rightarrow -193.4 \geq 5 - 1$ which is not true
    - $= \Rightarrow$MOSFET is not in saturation
    - Also note that $V_D = -193.4V$ is not possible in the given circuit as there is no -ve power supply present.
- Assume triode mode
  - $= \Rightarrow I_D = k_n\text{'}\frac{W}{L}\left[\left(V_{GS} - V_t\right)V_{DS} - \frac{1}{2}V_{DS}^2\right]$
    - $I_D = 1m\left[\left(4\right)V_{DS} - \frac{1}{2}V_{DS}^2\right]$
  - by ohm's law $I_D = \frac{V_{DD} - V_{DS}}{R_D} = \frac{5 - V_{DS}}{24.8k}$
  - eliminating I_D from the above two equations
    - $= \Rightarrow \frac{5 - V_{DS}}{24.8k} = 1m\left[4V_{DS} - \frac{1}{2}V_{DS}^2\right]$
    - $5 - V_{DS} = 24.8\left[4V_{DS} - \frac{1}{2}V_{DS}^2\right]$
    - $5 - V_{DS} = 99.2V_{DS} - \frac{24.8}{2}V_{DS}^2$
    - $5 - V_{DS} = 99.2V_{DS} - 12.4V_{DS}^2$
    - $12.4V_{DS}^2 + 5 - V_{DS} - 99.2V_{DS} = 0$
    - $12.4V_{DS}^2 - 100.2V_{DS} + 5 = 0$
    - $V_{DS} = V_D \because V_S = 0$
    - $V_{DS} = V_D = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} = \frac{100.2 \pm \sqrt{(-100.2)^2 - 4\left(12.4\right)\left(5\right)}}{2(12.4)}$
    - $= \Rightarrow V_D = 4.0403 \pm 3.9901 = 8.0304V\ ,\ 0.0502V$
    - $V_D = 8.0304V$ not possible $\because V_{DD} = +5V$ i.e. V_D can not exceed 5V
  - $= \Rightarrow V_D = 0.0502V$
  - $I_D = \frac{5 - V_{DS}}{24.8k} = \frac{5 - V_D}{24.8k} = \frac{5 - 0.0502}{24.8k} = 0.19959mA$
- now to verify the MOSFET is in triode region
  - $V_{DS} < V_{GS} - V_t$
  - or 0.0502<4 which is TRUE
  - $= \Rightarrow$MOSFET is indeed in triode region.



- Figure for Exercise 5.11

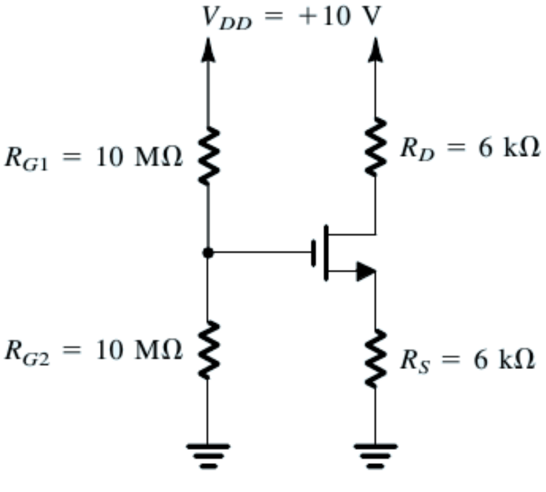
Exercise 5.11: (Approximate Analysis)

- Now R_D is doubled
  - $= \Rightarrow R_D = 2 \times 12.4k\Omega = 24.8k\Omega$
    - $I_D = \frac{V_{DD} - V_D}{R} = \frac{5 - V_D}{24.8k}$ ....(A)
    - Approximation comes from assuming that r_{DS} stays the same as before
    - i.e. $r_{DS} = \frac{V_{DS}}{I_D} = 253\Omega$
      - $= \Rightarrow I_D = \frac{V_{DS}}{r_{DS}} = \frac{V_D - V_S}{253} = \frac{V_D}{253}$ ....(B)
    - (A) and (B)
      - $= \Rightarrow \frac{5 - V_D}{24.8k} = \frac{V_D}{253} = \Rightarrow \frac{5}{24.8k} - \frac{V_D}{24.8k} = \frac{V_D}{253}$
      - $\frac{5}{24.8k} - \frac{V_D}{24.8k} = \frac{V_D}{253} = \Rightarrow \frac{5}{24.8k} = \frac{V_D}{253} + \frac{V_D}{24.8k}$
      - $V_D = \left(\frac{5}{24.8k}\right) / \left(\frac{1}{253} + \frac{1}{24.8k}\right) = 0.0505V$



    - Figure for Exercise 5.11
  - and from (A), $I_D = \frac{5 - V_D}{24.8k} = \frac{5 - 0.0505}{24.8k} = 0.19958mA$

Example 5.6

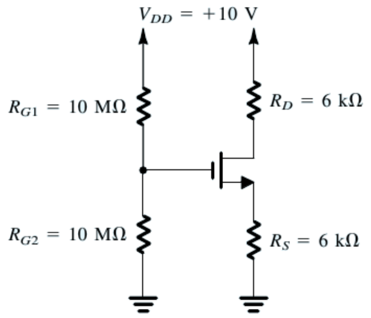
- Analyze the circuit shown in Fig. 5.24(a) to determine the voltages at all nodes and the currents through all branches. Let $V_{tn} = 1V$ and $k_n'(W / L) = 1mA/V^2$. Neglect the channel-length modulation effect (i.e., assume $\lambda = 0$).
  - 

(a)

Solution: Example 5.6

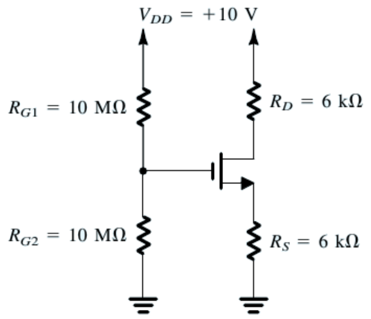
- here
  - $V_{tn} = 1V$, $k_n'(W / L) = 1mA/V^2$, $\lambda = 0$
    - as no current flows into the gate terminal
    - by voltage divider
      - $v_G = \frac{R_{G2}}{R_{G1} + R_{G2}} V_{DD} = \frac{10M}{20M}\left(10\right) = 5V$

            - $I_{R_{G1}} = I_{R_{G2}} = \frac{v_G - 0}{R_{G2}} = \frac{5}{10M} = 0.5\mu A$
        - As a +ve gate voltage exists, it is expected
            - $= \Rightarrow$the transistor is ON
        - however, we dont know whether it is operating in triode or saturation region



(a)

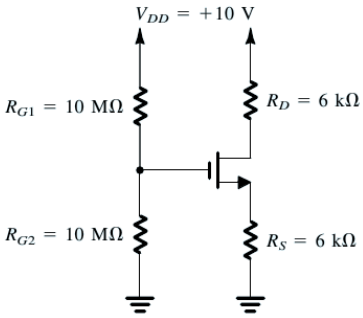
- let's solve by assuming the NMOS transistor is operating in saturation region,
    - and then check the validity of our assumption.
        - if our assumpltion turns out to be invalid,
            - we will have to solve the problem again for the triode region of operation.
        - thus for saturation region,
            - $i_D = \frac{1}{2} k_n{'} \left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2$
            - $I_D = \frac{1}{2}\left(1m\right)(V_G - V_S - V_{tn})^2$
            - $I_D = 0.5m(5 - V_S - 1)^2$
            - $I_D = 0.5m(4 - V_S)^2$



(a)

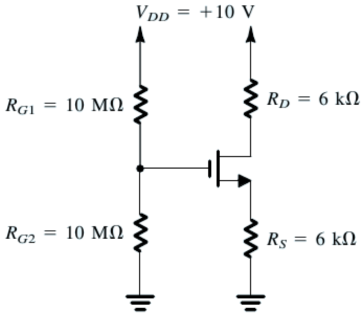
- $I_D = 0.5m(4 - V_S)^2$
    - also $I_D = \frac{V_S - 0}{6k} = \frac{V_S}{6k} = \Rightarrow V_S = (6k) I_D$
        - substitute V_S into above expression for I_D
            - $= \Rightarrow I_D = 0.5m(4 - V_S)^2 = 0.5m(4 - (6k)I_D)^2$
            - $I_D = 0.5m\left(16 + \left(36M\right) I_D^2 - 2\left(4\right)\left(6k\right) I_D\right)$
            - $I_D = 0.5m\left(16 + \left(36M\right) I_D^2 - 2\left(4\right)\left(6k\right) I_D\right)$
            - $I_D = 8m + \left(18k\right) I_D^2 - 24 I_D$
            - $25 I_D = 8m + \left(18k\right) I_D^2$
            - $\left(18k\right) I_D^2 - 25 I_D + 8m = 0$
        - this quadratic equation has the solution of

- $I_D = \frac{-b \pm \sqrt{b^2-4ac}}{2a} = \frac{25 \pm \sqrt{(25)^2 - 4\left(18k\right)\left(8m\right)}}{2(18k)}$
- $I_D = \frac{25 \pm 7}{36k} = 0.89mA\ ,\ 0.5mA$



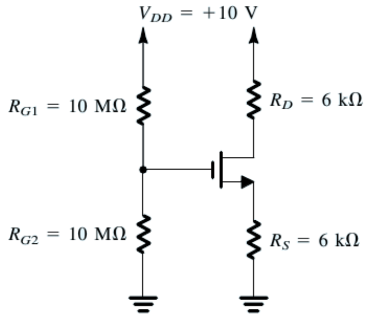
(a)

- $I_D = \frac{25 \pm 7}{36k} = 0.89mA\ ,\ 0.5mA$
  - As $V_S = (6k) I_D$
    - $= \Rightarrow V_S = 5.34V$ for $I_D = 0.89mA$
      - and $V_S = 3V$ for $I_D = 0.5mA$
    - Note that for $V_S = 5.34V$ ($I_D = 0.89mA$) $= \Rightarrow V_{GS} = 5 - 5.34 = -0.34$
      - $= \Rightarrow$ the MOSFET is off, so no I_D can't be equal to 0.89mA
      - thus this case is invalid
    - $= \Rightarrow V_S = 3V$ and $I_D = 0.5mA$
      - $V_{GS} = 5 - 3 = 2V$
      - $V_{GS} - V_{tn} = 2 - 1 = 1V$



(a)

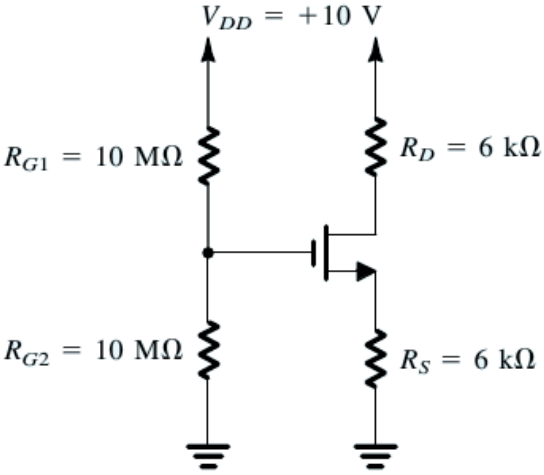
- As $I_D = \frac{V_{DD} - V_D}{R_D} = \frac{10 - V_D}{6k}$
  - $= \Rightarrow I_D = \frac{V_{DD} - V_D}{R_D} = \frac{10 - V_D}{6k}$
    - $0.5m = \frac{10 - V_D}{6k}$
      - $3 = 10 - V_D = \Rightarrow V_D = 10 - 3 = 7V$
    - $V_{DS} = V_D - V_S = 7 - 3 = 4V$
    - $= \Rightarrow$ here $V_{DS} = 4V$, $V_{GS} - V_t = 2 - 1 = 1V$
      - $= \Rightarrow V_{DS} > V_{GS} - V_t$
      - i.e. $4V > 1V$
      - $= \Rightarrow$ the initial assumption was correct, the transistor is in saturation region.



(a)

Exercise 5.12

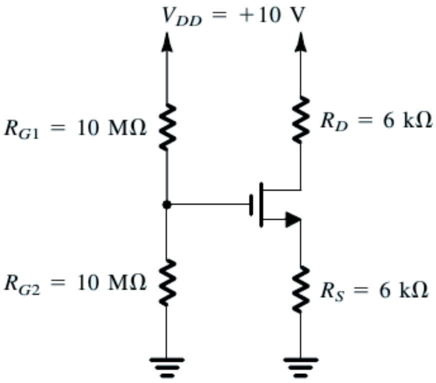
- For the circuit of Fig. 5.24, what is the largest value that R_D can have while the transistor remains in the saturation mode?



  - (a)

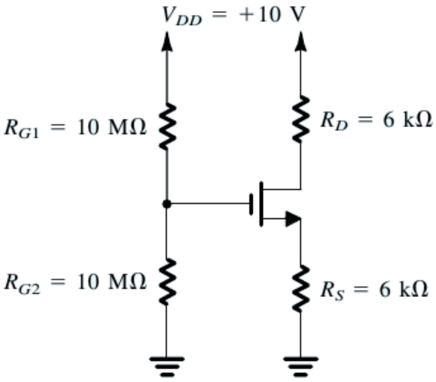
Solution: Exercise 5.12

- for Saturation mode
  - $v_{DS} \geq v_{GS} - V_t$
    - or $v_D \geq v_G - V_t$
    - for $\lambda = 0$, I_D remains constant in saturation region w.r.t v_{DS}
      - as $R_D = \frac{V_{DD} - V_D}{I_D}$
      - R_D is largest when V_D is smallest. As V_{DD} and I_D are constants.
    - $= \Rightarrow R_D = ?$ when $V_D = V_G - V_t = 5 - 1 = 4V$
      - $R_D = \frac{V_{DD} - V_D}{I_D} = \frac{10-4}{I_D} = \frac{6}{I_D}$
    - where $i_D = \frac{1}{2} k_n\text{'} \left(\frac{W}{L}\right) (v_{GS} - V_{tn})^2$



(a)

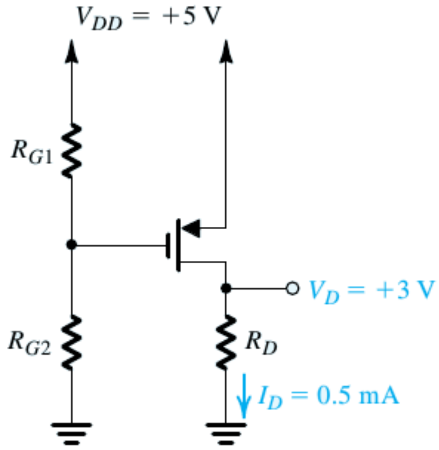
- $i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2$
  - As R_S has not changed, $= \Rightarrow v_{GS}$ is not changed
    - $I_D = 0.5m(V_G - V_S - 1)^2 = 0.5m(5 - V_S - 1)^2 = 0.5m(4 - V_S)^2$
      - also $I_D = \frac{V_S - 0}{6k} = \Rightarrow V_S = I_D 6k$
      - these two equations have already been solved in Example 5.6
      - $= \Rightarrow I_D = 0.5mA$
    - $= \Rightarrow R_D = \frac{6}{I_D} = \frac{6}{0.5m} = 12k\Omega$



(a)

Example 5.7

- Design the circuit of Fig. 5.25 so that the transistor operates in saturation with $I_D = 0.5mA$ and $V_D = +3V$. Let the enhancement-type PMOS transistor have $V_{tp} =-1V$ and $kp'(W\ /\ L) = 1mA/V^2$. Assume $\lambda = 0$. What is the largest value that R_D can have while maintaining saturation-region operation?



- **Figure 5.25** Circuit for Example 5.7.

Solution: Example 5.7

- here
  - saturation region and $I_D = 0.5mA$
    - $V_{tp} = -1V$, $k_p'\left(\frac{W}{L}\right) = 1m\frac{A}{V^2}$, $\lambda = 0$
    - in saturation region
      - $i_D = \frac{1}{2}k_p'\left(\frac{W}{L}\right)(v_{SG} - |V_{tp}|)^2$
      - $0.5m = \frac{1}{2}\left(1m\right)(v_{SG} - 1)^2$
      - $0.5m = \left(0.5m\right)(v_{SG} - 1)^2$
      - $(v_{SG} - 1)^2 = 1 = \Rightarrow v_{SG} - 1 = \pm 1$
      - or $v_{SG} = 1 \pm 1 = 2$, 0
      - $v_{SG} = 0$ doesnot make any sense as it means the device is cutoff but the given $I_D = 0.5mA$, so the device cannot be cutoff
    - $= \Rightarrow V_{SG} = 2V$

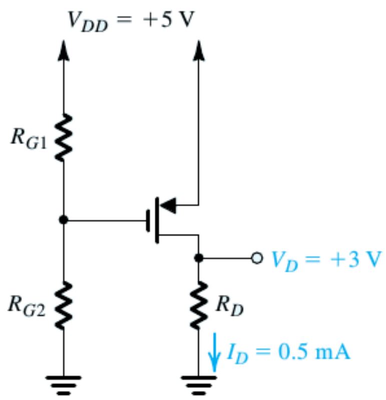


Figure 5.25 Circuit for Example 5.7.

- $V_{SG} = 2V$
  - $V_S - V_G = 2V$
    - or $5 - V_G = 2V$
      - $V_G = 5 - 2 = 3V$
    - from the figure
      - $V_G = \frac{R_{G2}}{R_{G1}+R_{G2}}V_{DD}$ and $\frac{5}{I_{R_{G1}}} = R_{G1} + R_{G2}$

- for $I_{R_{G1}} = 1\mu A = \Rightarrow R_{G1} + R_{G2} = \frac{5}{1\mu} = 5M\Omega$
- $V_G = \frac{R_{G2}}{R_{G1}+R_{G2}} V_{DD} = \Rightarrow \frac{3}{5} = \frac{R_{G2}}{R_{G1}+R_{G2}} = \frac{R_{G2}}{5M} = \Rightarrow$ $R_{G2} = \frac{3}{5} \times 5M = 3M\Omega$
- $R_{G1} = 5M - R_{G2} = 2M\Omega$

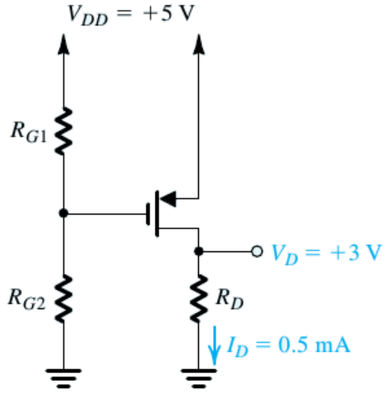


Figure 5.25 Circuit for Example 5.7.

- for saturation
  - $v_{SD} \geq v_{SG} - |V_{tp}|$
    - $v_S - v_D \geq v_S - v_G - |V_{tp}|$
      - $-v_D \geq -v_G - |V_{tp}|$
      - $-v_D \geq -v_G - 1$
      - $v_D \leq v_G + 1$
    - at the edge (i.e. at the start of saturation region)
      - $v_D = v_G + 1 = 3 + 1 = 4V$
      - $= \Rightarrow R_D = \frac{V_D - 0}{I_D} = \frac{4-0}{0.5m} = 8k\Omega$

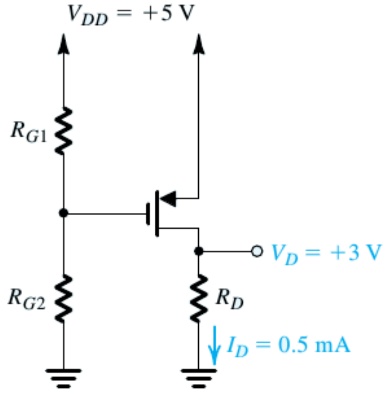


Figure 5.25 Circuit for Example 5.7.