Lecture 6a

EE-215 Electronic Devices and Circuits

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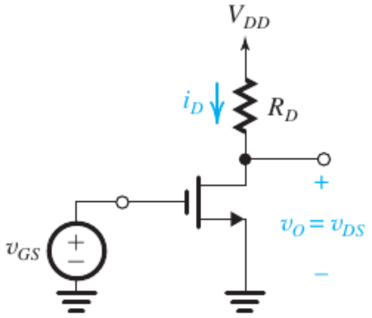
Applying the MOSFET in Amplifier Design

- When operated in saturation, the MOSFET acts as a voltage-controlled current source.
    - this enables us to use the MOSFET in the design of amplifiers

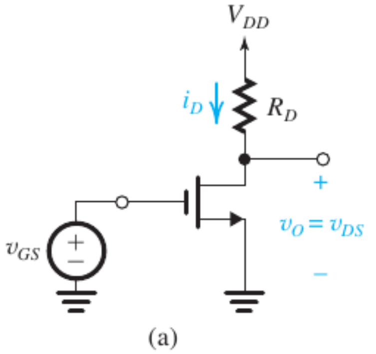
Obtaining a Voltage amplifier

- A voltage controlled current source can be used as a transconductance amplifier
    - A transconductance amplifier is an amplifier whose input signal is a voltage and output signal is a current
        - we usually are more interested in a voltage amplifier
        - A transconductance amplifier can be converted into a voltage amplifier,
            - by passing the output current through a resistor
            - and taking the voltage across the resistor as output

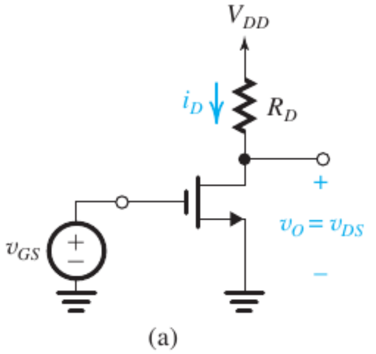


(a)

- in the figure
    - v_{GS} is the input voltage
        - R_D is called the load resistance.
            - R_D converts the drain current i_D to a voltage $i_D R_D$
            - V_{DD} is the supply voltage
        - here the output voltage is taken between the drain terminal and the ground (rather than across R_D)
            - this arrangement enables us to maintain a ground reference through out the circuit
            - $= \Rightarrow$
            - v_{GS} is the input voltage
            - v_{DS} is the output voltage



- Using KVL, an expression for v_{DS} can be computed
    - i.e. $V_{DD} = i_D R_D + v_{DS}$
        - or $v_{DS} = V_{DD} - i_D R_D$
        - $= \Rightarrow$ output voltage v_{DS} is an inverted version of $i_D R_D$ that is shifted by the constant value of the supply voltage V_{DD}



The Voltage Transfer Characteristic (VTC)

- VTC is a plot of the output voltage versus the input voltage
    - and it can provide a better insight in to the operation of an amplifier circuit

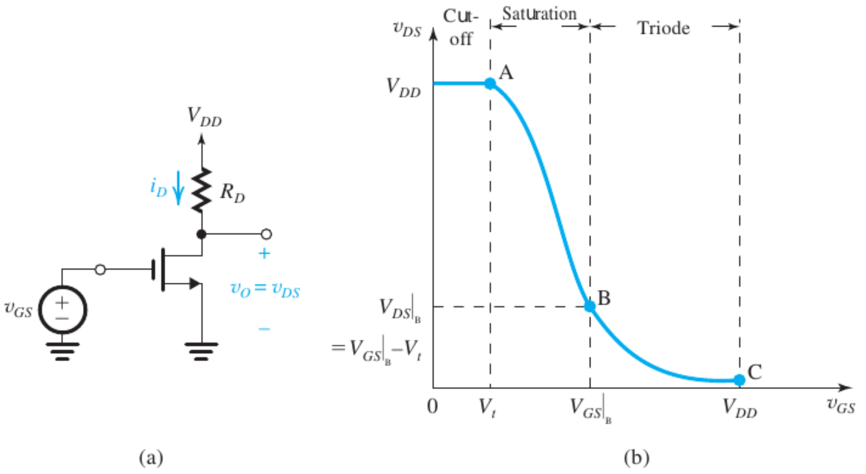
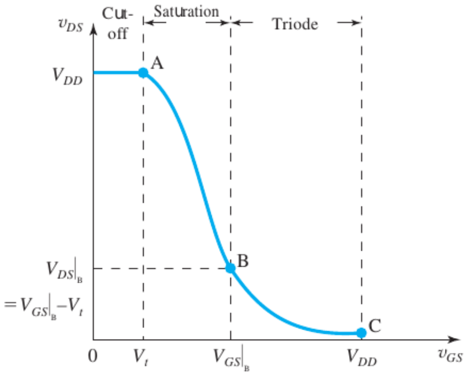


Figure 5.27 **(a)** Simple MOSFET amplifier with input v_{GS} and output v_{DS}. **(b)** The voltage transfer characteristic (VTC) of the amplifier in **(a)**. The three segments of the VTC correspond to the three regions of operation of the MOSFET.

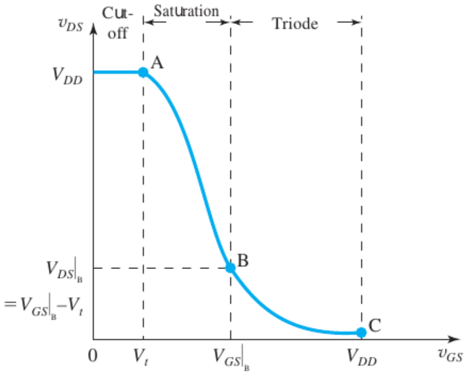
- Note that for $v_{GS} < V_t$, the transistor is cut-off $= \Rightarrow i_D = 0$
    - and $v_{DS} = V_{DD} - i_D R_D = V_{DD}$
        - As v_{GS} exceeds V_t, the transistor turns on and v_{DS}

    decreases.
      - As initially i_D is still small
      - $= \Rightarrow v_{DS}$ is still high
      - $= \Rightarrow$ MOSFET is operating in saturation region



(b)

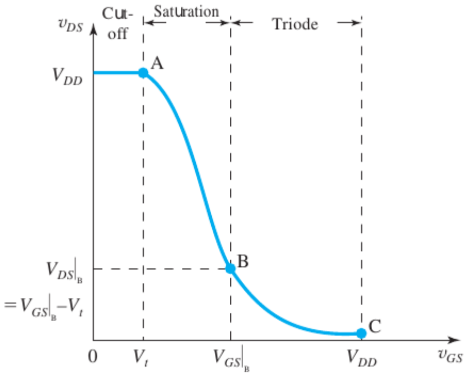
  - MOSFET stays in saturation region as v_{GS} is increased
    - untill the value of v_{GS} is reached for which $v_{DS} = v_{GS} - V_t$
    - this is point B
  - for $v_{DS} < v_{GS} - V_t$ (i.e. beyond point B), the transistor enters the triode region,
- from the fig, it is clear that the segment of greatest slope
  - (and hence the largest amplifier gain) is that labeled as AB
    - which corresponds to the saturation region of operation
  - thus for amplifier application, one will always choose to operate the MOSFET in saturation region
    - Also note from VTC, that for digital circuit applications, we operate the MOSFET as switch in cutoff and triode regions.
      - MOSFET acts as an off switch in cutoff region
      - and as an ON switch in triode region



(b)

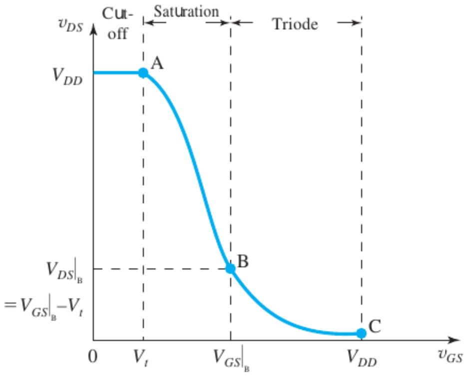
  - Cutoff $= \Rightarrow v_{DS} = V_{DD}$ and Triode $= \Rightarrow v_{DS} \approx 0$
- So as a digital circuit,
  - this circuit acts as a logic inverter

        - i.e. for $v_{IN} = v_{GS} = V_{DD} = \Rightarrow v_{OUT} = v_{DS} = 0V$
            - and for $v_{IN} = v_{GS} = 0V$ $= \Rightarrow v_{OUT} = v_{DS} = V_{DD}$



(b)

- Now for amplifier application, the MOSFET will be operated in saturation region i.e. in the segment AB
    - for saturation region operation (ignoring channel length modulation i.e. for $\lambda = 0$)
        - $i_D = \frac{1}{2} k_n' \frac{W}{L} (v_{GS} - V_t)^2 = \frac{1}{2} k_n (v_{GS} - V_t)^2$
        - where k_n is the MOSFET transconductance parameter
    - As $v_{DS} = V_{DD} - i_D R_D$
        - $v_{DS} = V_{DD} - i_D R_D = V_{DD} - \left[\frac{1}{2} k_n (v_{GS} - V_t)^2\right] R_D$
    - $v_{DS} = V_{DD} - \frac{1}{2} k_n R_D (v_{GS} - V_t)^2$
- $v_{DS} = V_{DD} - \frac{1}{2} k_n R_D (v_{GS} - V_t)^2$
    - Let's determine the co-ordinates of point B
        - As point B is at the boundary between the saturation and the triode regions of operation
        - $= \Rightarrow v_{GS} = .\, V_{GS}|_B$
            - $v_{DS} = .\, V_{DS}|_B = .\, V_{GS}|_B - V_t$



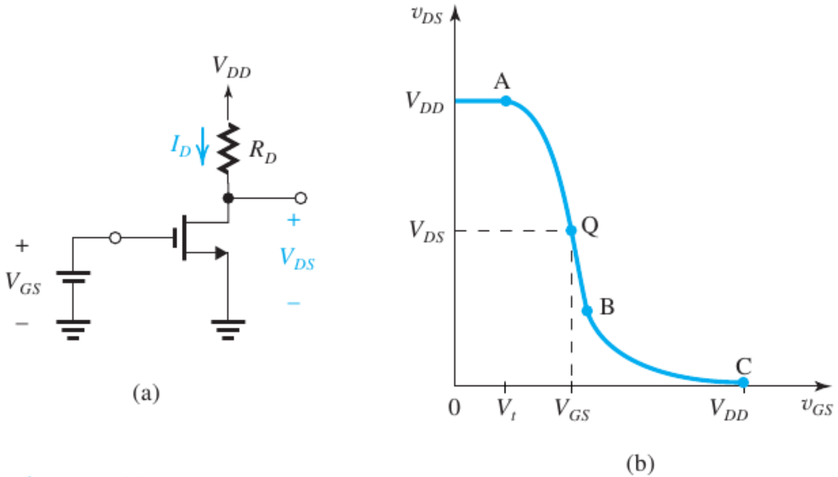
(b)

    - or $V_{DD} - \frac{1}{2} k_n R_D (.\, V_{GS}|_B - V_t)^2 = .\, V_{GS}|_B - V_t$
    - Rearranging

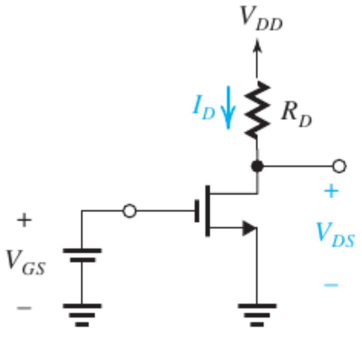
        - $-\frac{1}{2}k_nR_D(.\,V_{GS}|_B - V_t)^2 - \left(.\,V_{GS}|_B - V_t\right) + V_{DD} = 0$
        - $\frac{1}{2}k_nR_D(.\,V_{GS}|_B - V_t)^2 + \left(.\,V_{GS}|_B - V_t\right) - V_{DD} = 0$
- $\frac{1}{2}k_nR_D(.\,V_{GS}|_B - V_t)^2 + \left(.\,V_{GS}|_B - V_t\right) - V_{DD} = 0$
    - $\left(.\,V_{GS}|_B - V_t\right) = \frac{-b\pm\sqrt{b^2-4ac}}{2a}$
        - $\left(.\,V_{GS}|_B - V_t\right) = \frac{-1\pm\sqrt{1^2-4\left(\frac{1}{2}k_nR_D\right)\left(-V_{DD}\right)}}{2\left(\frac{1}{2}k_nR_D\right)}$
        - $\left(.\,V_{GS}|_B - V_t\right) = \frac{-1\pm\sqrt{1+2k_nR_DV_{DD}}}{k_nR_D} = \frac{\pm\sqrt{1+2k_nR_DV_{DD}}-1}{k_nR_D}$
    - As $(.\,V_{GS}|_B - V_t)$ has to be +ve at point B
        - $\because$ the device is on at B (and as k_n , R_D, V_{DD} are +ve values)
    - $= \Rightarrow \left(.\,V_{GS}|_B - V_t\right) = \frac{+\sqrt{1+2k_nR_DV_{DD}}-1}{k_nR_D}$
    - or $.\,V_{GS}|_B = V_t + \frac{\sqrt{1+2k_nR_DV_{DD}}-1}{k_nR_D}$

Biasing the MOSFET to Obtain Linear Amplification

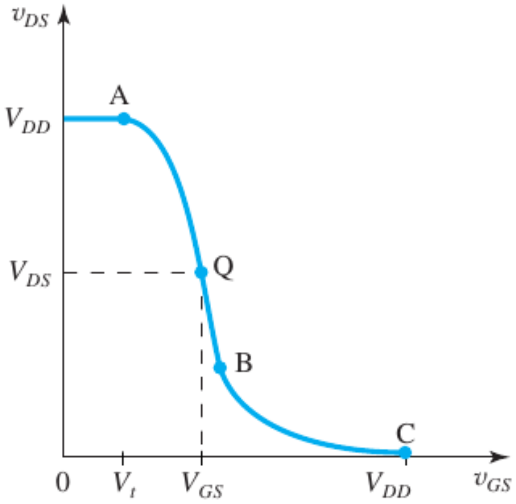
- Biasing enables us to obtain almost-linear amplification from the MOSFET



    - **Figure 5.28** Biasing the MOSFET amplifier at a point Q located on the segment AB of the VTC.
    - A dc voltage V_{GS} is selected to obtain operation at a point Q on the segment AB
- the resulting V_{DS} can be given as
    - $V_{DS} = V_{DD} - \frac{1}{2}k_nR_D(V_{GS} - V_t)^2$
        - Point Q is called the bias point
            - or the dc operating point
            - or the Quiescent point

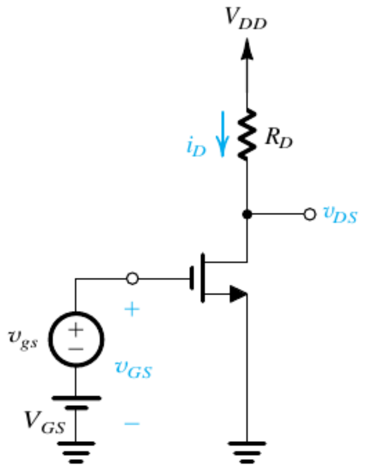


(a)



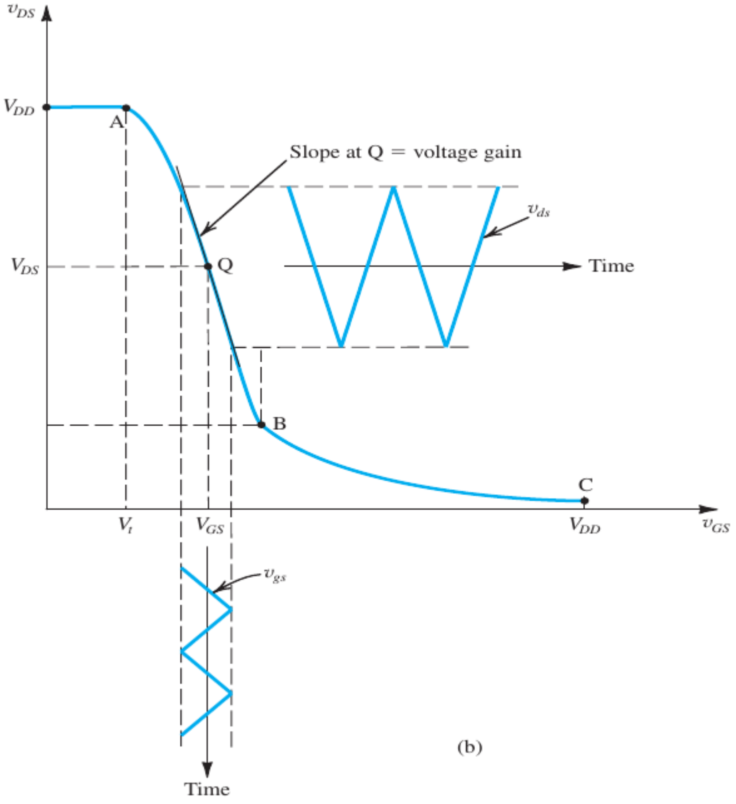
(b)

- Once the Q point is selected, the ac signal to be amplified is superimposed on the bias voltage V_{GS}
    - $= \Rightarrow$ the total instantaneous value of v_{GS} is
        - $v_{GS}(t) = V_{GS} + v_{gs}(t)$
    - the resulting v_{DS} is
        - $v_{DS}\left(t\right) = V_{DD} - \frac{1}{2}k_n R_D (v_{GS} - V_t)^2$



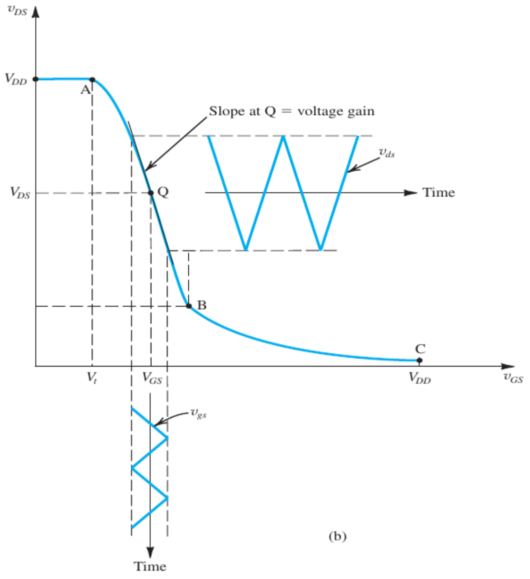
(a)

- $v_{DS}(t)$ can also be obtained graphically from the VTC
    - Note that if the amplitude of v_{gs} is small enough to
        - restrict the signal swing to a short almost-linear segment
            - of the VTC, linear amplification is achieved
        - The shorter the segment, the greater the linearity achieved.

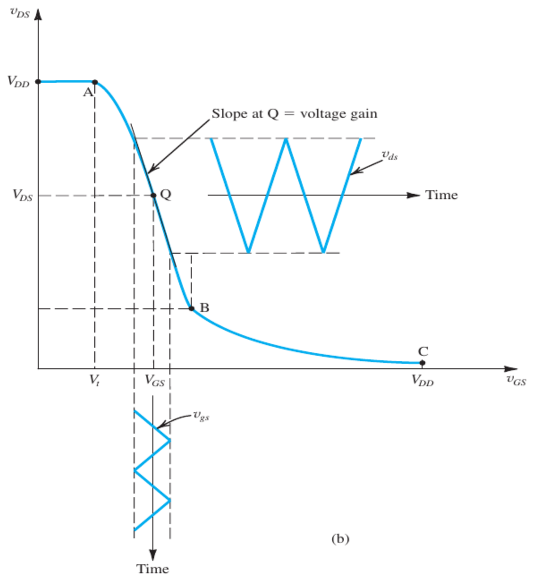


The Small-Signal Voltage Gain

- if the input signal v_{gs} is kept small, the output signal v_{ds} is nearly proportional to v_{gs}
    - i.e. $v_{ds} \propto v_{gs}$
        - or $v_{ds} = A_v v_{gs}$
        - A_v is the proportionality constant and is the voltage gain of the amplifier
        - A_v is the slope of the almost linear segment of the VTC around Q
            - i.e. $A_v = . \left.\frac{\partial v_{DS}}{\partial v_{GS}}\right|_{v_{GS}=V_{GS}}$



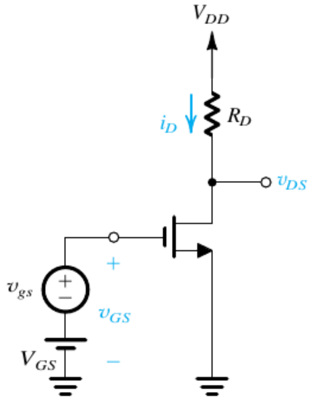
- $A_v = .\ \frac{\partial v_{DS}}{\partial v_{GS}}\Big|_{v_{GS}=V_{GS}}$
    - using $v_{DS}\left(t\right) = V_{DD} - \frac{1}{2}k_n R_D (v_{GS} - V_t)^2$
        - $A_v = .\ \frac{\partial}{\partial v_{GS}}\left[V_{DD} - \frac{1}{2}k_n R_D (v_{GS} - V_t)^2\right]\Big|_{v_{GS}=V_{GS}}$
        - $A_v = .\ 0 - \frac{1}{2}k_n R_D 2\left(v_{GS} - V_t\right)\frac{\partial}{\partial v_{GS}}\left[v_{GS} - V_t\right]\Big|_{v_{GS}=V_{GS}}$
        - $A_v = .\ -k_n R_D (v_{GS} - V_t)(1)\big|_{v_{GS}=V_{GS}}$
        - $A_v = -k_n R_D (V_{GS} - V_t)$
    - $A_v = -k_n (V_{GS} - V_t) R_D = -k_n V_{OV} R_D$
- $A_v = -k_n (V_{GS} - V_t) R_D = -k_n V_{OV} R_D$
    - from this expression, Note that
        1. The voltage gain is negative
            - $= \Rightarrow$the amplifier is inverting.
            - i.e . there is a 180^o phase shift between the input and the output
            - this inversion is clear from the figure
        2. The gain is proportional to the load resistance R_D,
            - to the overdrive voltage v_{OV}
            - and to the transistor transconductance parameter k_n



- $A_v = -k_n(V_{GS} - V_t)R_D = -k_n V_{OV} R_D$
  - As the dc drain current I_D(at the bias point Q) can be given as
    - $I_D = \frac{1}{2}k_n'\frac{W}{L}(V_{GS} - V_t)^2 = \frac{1}{2}k_n(V_{OV})^2$
      - or $k_n V_{OV} = \frac{2I_D}{V_{OV}}$
  - $= \Rightarrow A_v = -k_n V_{OV} R_D = -\frac{2I_D}{V_{OV}}R_D = -\frac{I_D R_D}{V_{OV}/2}$
    - thus the gain is simply the ratio of the dc voltage drop across the load resistor R_D to $V_{OV}/2$
  - this relation is useful in determining the absolute upper limit on the magnitude of voltage gain for this amplifier circuit
  - Note that
    - $I_D R_D$ is the voltage drop across the resistor R_D. this voltage drop can approach but never exceed the power-supply voltage V_{DD}
    - $= \Rightarrow \left|A_{v_{max}}\right| = \frac{V_{DD}}{V_{OV}/2}$

Example 5.9

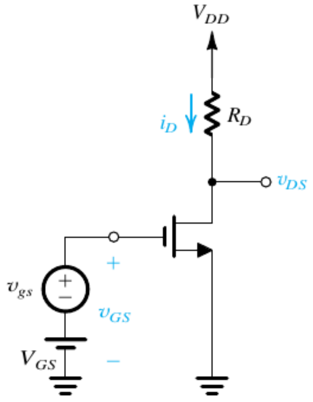
- Consider the amplifier circuit shown in Fig. 5.29(a). The transistor is specified to have $V_t = 0.4V$, $k_n' = 0.4mA/V_2$, $W/L = 10$, and $\lambda = 0$. Also, let $V_{DD} = 1.8V$, $R_D = 17.5k\Omega$, and $V_{GS} = 0.6V$.
  - (a) For $v_{gs} = 0$ (and hence $v_{ds} = 0$), find V_{OV}, I_D , V_{DS} , and A_v.
    - (b) What is the maximum symmetrical signal swing allowed at the drain? Hence find the maximum allowable amplitude of a sinusoidal v_{gs}.



(a)

Example 5.9(a)

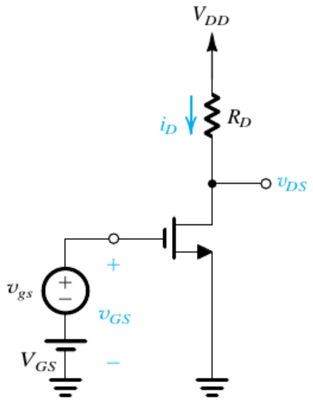
- $V_t = 0.4V$, $k_n' = 0.4mA/V_2$, $W/L = 10$, and $\lambda = 0$.
  - $V_{DD} = 1.8V$, $R_D = 17.5k\Omega$, and $V_{GS} = 0.6V$.
  - $v_{gs} = 0$
    - V_{OV} =?, I_D =? , V_{DS} =? , and A_v =?.
    - $V_{OV} = V_{GS} - V_t = 0.6 - 0.4 = 0.2V$
    - Assuming saturation region of operation
      - $I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2$
      - $I_D = \frac{1}{2} \left(0.4m\right) \left(10\right) (0.2)^2 = 80\mu A$
    - by KVL
      - $V_{DD} = I_D R_D + V_{DS}$
      - $V_{DS} = V_{DD} - I_D R_D$
      - $V_{DS} = 1.8 - (80\mu)(17.5k) = 0.4V$



(a)

- for saturation
  - $V_{DS} > V_{GS} - V_t$
    - $0.4 > 0.6 - 0.4$
      - $0.4 > 0.2$ which is true $= \Rightarrow$the mosfet is in saturation. our initial assumption was correct.
    - the voltage gain A_v is

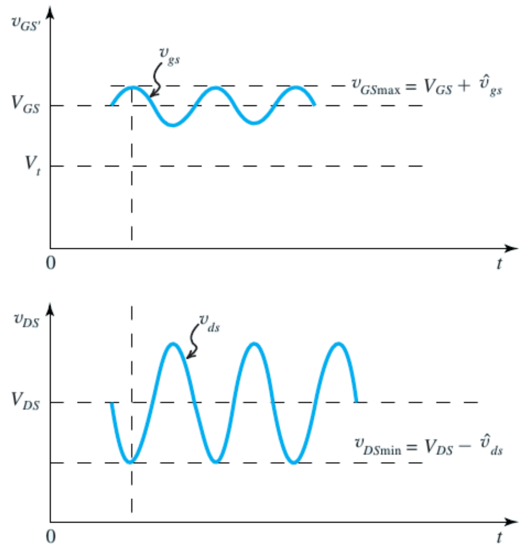
- $A_v = -k_n V_{OV} R_D$
- $A_v = -k_n{}' \frac{W}{L} V_{OV} R_D$
- $A_v = -\left(0.4m\right)\left(10\right)\left(0.2\right)\left(17.5k\right) = -14\frac{V}{V}$



(a)

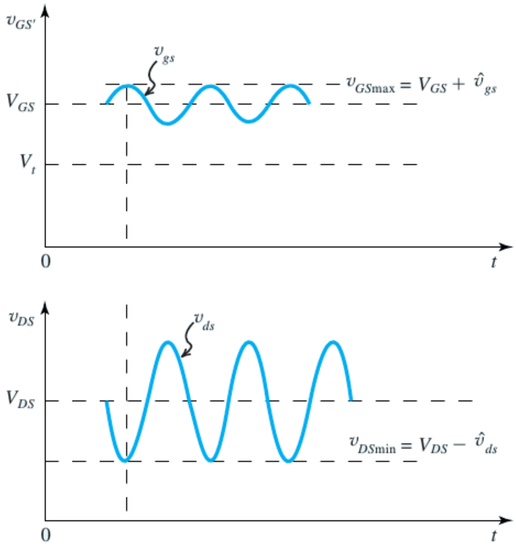
Example 5.9(b)

- to ensure the transistor is in saturation region (segment AB on VTC)
    - $v_{DS} \geq v_{GS} - V_t$ and $v_{GS} \geq V_t$
        - the first avoids triode region and 2nd avoids cut-off region
        - from the figure (as the output is 180^o out of phase relative to input)
            - $v_{DS_{min}} \geq v_{GS_{max}} - V_t$ and $v_{GS_{min}} \geq V_t$

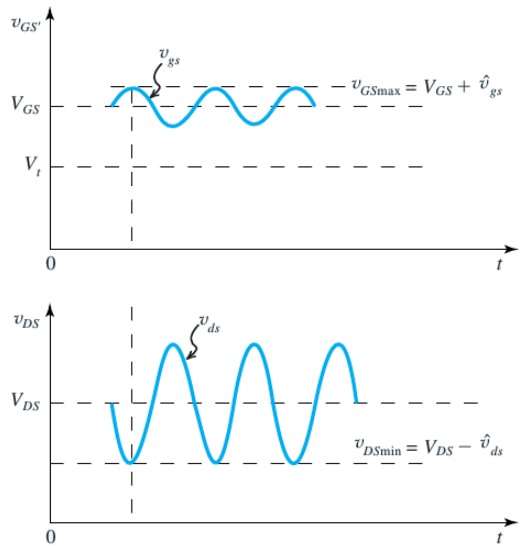


- $v_{DS_{min}} \geq v_{GS_{max}} - V_t$
    - $V_{DS} - \hat{v}_{ds} \geq (V_{GS} + \hat{v}_{gs}) - V_t$
        - $0.4 - \hat{v}_{ds} \geq (0.6 + \hat{v}_{gs}) - 0.4 \because V_{DS} = 0.4$, $V_{GS} = 0.6$, $V_t = 0.4$
            - $0.4 - \hat{v}_{ds} \geq 0.6 + \hat{v}_{gs} - 0.4$
            - $0.4 - \hat{v}_{ds} \geq 0.2 + \hat{v}_{gs}$
            - $0.2 - \hat{v}_{ds} \geq \hat{v}_{gs}$

        - As $\frac{v_{ds}}{v_{gs}} = A_v = -14$
        - As the -ve sign of A_v has already been accomodated in fig
            - $= \Rightarrow \hat{v}_{ds} = |A_v| \hat{v}_{gs} = 14\hat{v}_{gs}$
        - substituting in to $0.2 - \hat{v}_{ds} \geq \hat{v}_{gs}$
            - $= \Rightarrow 0.2 - 14\hat{v}_{gs} \geq \hat{v}_{gs}$



- $0.2 - 14\hat{v}_{gs} \geq \hat{v}_{gs}$
    - $0.2 \geq 15\hat{v}_{gs}$
        - $\hat{v}_{gs} = \frac{0.2}{15} = 13.33mV$
            - for +ve swing $\hat{v}_{gs} \leq 13.33mV$
        - To avoid cut-off region $v_{GS_{min}} \geq V_t$
            - $V_{GS} - \hat{v}_{gs} \geq V_t$
            - $0.6 - \hat{v}_{gs} \geq 0.4 \because V_{GS} = 0.6, V_t = 0.4$
            - $-\hat{v}_{gs} \geq -0.2$
            - $\hat{v}_{gs} \leq 0.2$
            - $\hat{v}_{gs} = 0.2V$
            - for -ve swing $\hat{v}_{gs} \leq 0.2V$



  - thus $\hat{v}_{gs} \leq 13.33mV$ to avoid signal clipping on both +ve and -ve swing

Determining the VTC by Graphical Analysis

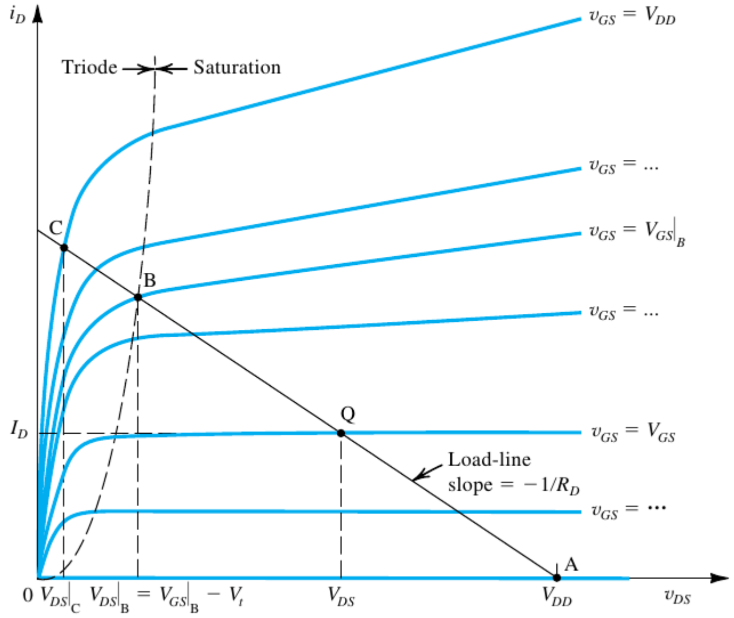
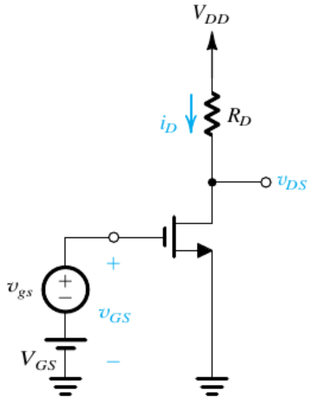
- Voltage transfer characteristic (VTC) of the amplifier can be determined using graphical method
  - 

Figure 5.31 Graphical construction to determine the voltage transfer characteristic of the amplifier in Fig. 5.29(a).



(a)

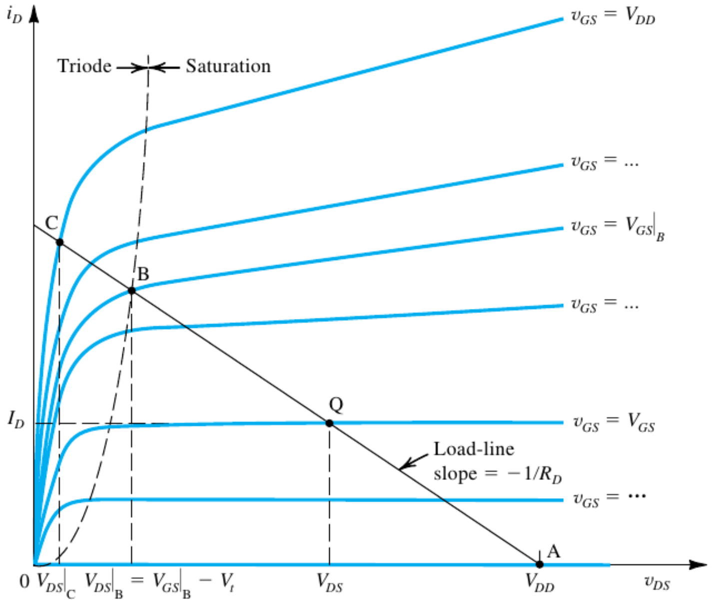
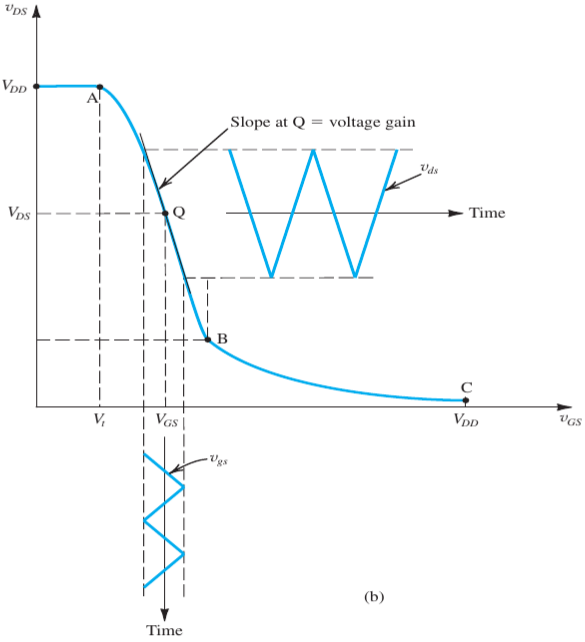


Figure 5.31 Graphical construction to determine the voltage transfer characteristic of the amplifier in Fig. 5.29(a).



(b)

- the graphical analysis is based on the fact that
    - for each value of v_{GS}, the circuit will be operating
        - at the point of intersection of the $i_D - v_{DS}$ graph

            - corresponding to that particular value of v_{GS}
            - and the straight line representing the KVL eq
            - i.e. $v_{DS} = V_{DD} - i_D R_D = \Rightarrow i_D = \frac{V_{DD}}{R_D} - \frac{v_{DS}}{R_D}$

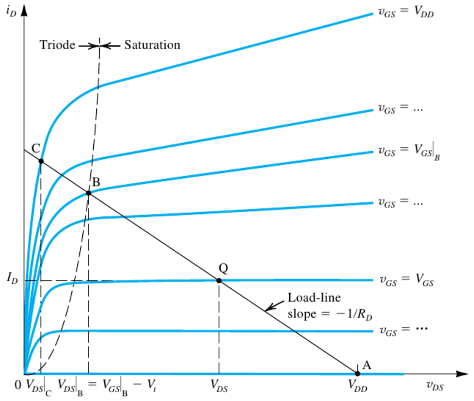


Figure 5.31 Graphical construction to determine the voltage transfer characteristic of the amplifier in Fig. 5.29(a).

    - The straight line representing this relationship is superimposed on the $i_D - v_{DS}$ characteristic

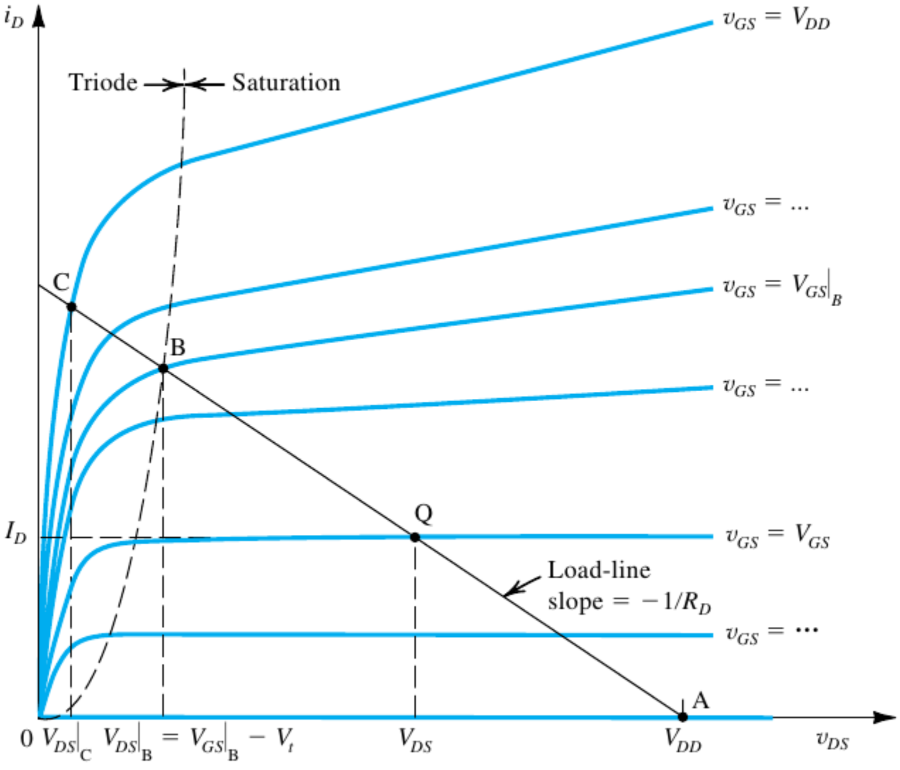


Figure 5.31 Graphical construction to determine the voltage transfer characteristic of the amplifier in Fig. 5.29(a).

- this line intersects the horizontal axis at $v_{DS} = V_{DD}$ and has a slope of $-\frac{1}{R_D}$
    - this line is called the load line as it represents the load resistance R_D
        - the VTC can then be determined point by point
            - here four important points have been labeled
        - At point A

         - $v_{GS} = V_t$
      - At point Q
         - MOSFET can be biased for amplifier application i.e. $v_{GS} = V_{GS}$, $v_{DS} = V_{DS}$

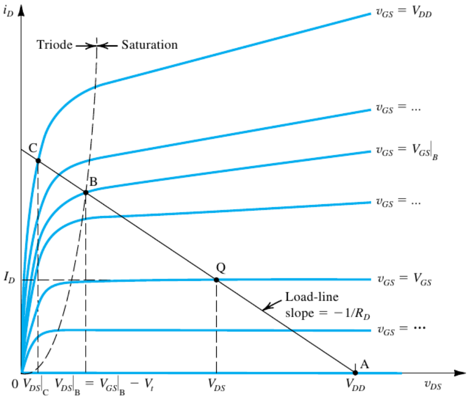


Figure 5.31 Graphical construction to determine the voltage transfer characteristic of the amplifier in Fig. 5.29(a).

- At point B,
   - the MOSFET leaves the saturation region and enters the triode region
      - At point C,
         - the MOSFET is deep into the triode region and $v_{GS} = V_{DD}$ at this point C
      - Note that if the MOSFET is to be used as a switch, then operating points A and C are applicable
         - At A, the transistor is off (open switch)
         - and at C the transistor operates as a low value resistance r_{DS} and has a small voltage drop (closed switch)

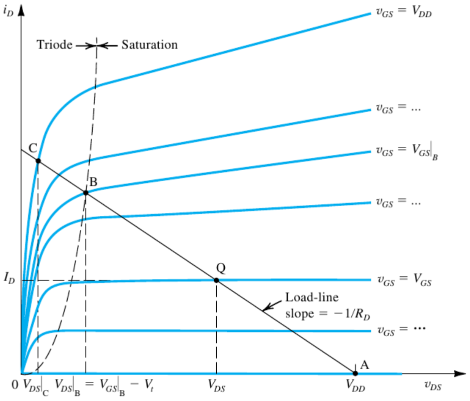


Figure 5.31 Graphical construction to determine the voltage transfer characteristic of the amplifier in Fig. 5.29(a).

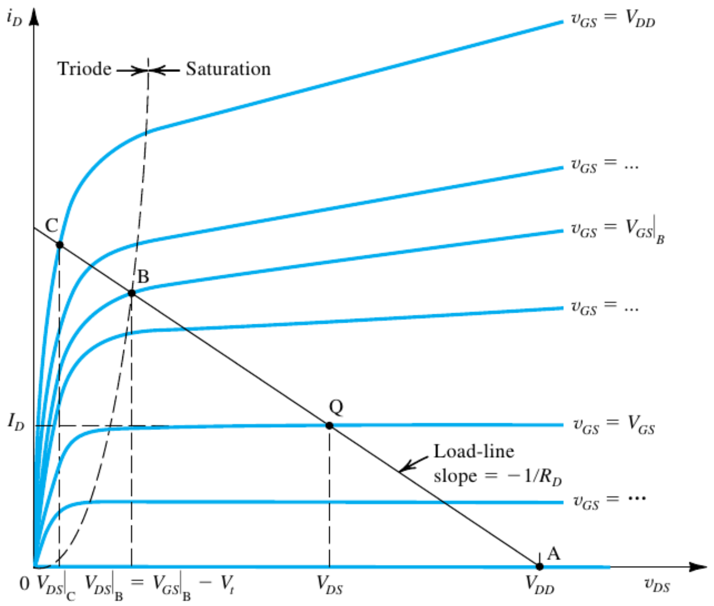
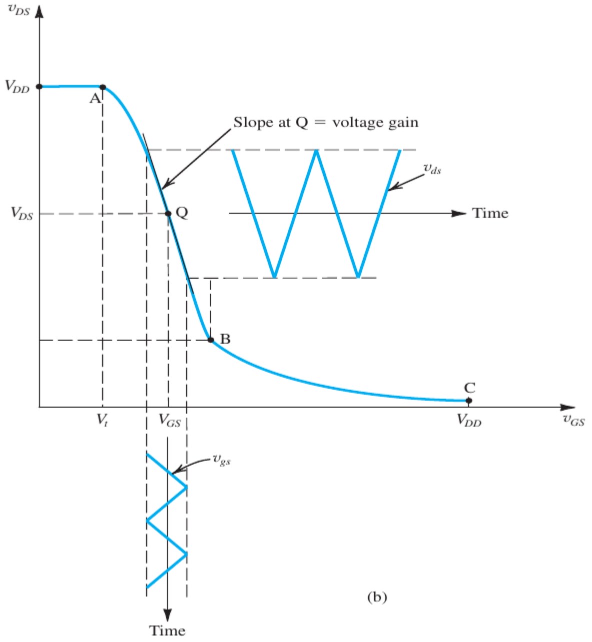


Figure 5.31 Graphical construction to determine the voltage transfer characteristic of the amplifier in Fig. 5.29(a).



(b)

Locating the Bias Point Q

- The bias point Q is determined by the value of v_{GS} and that of the load resistance R_D
    - Two important considerations in choosing the location of Q are
        - the required gain and
            - the allowable signal swing at the output

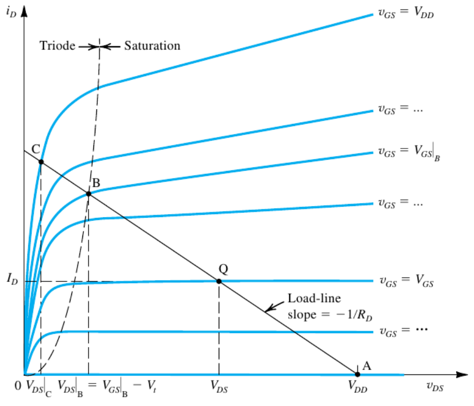
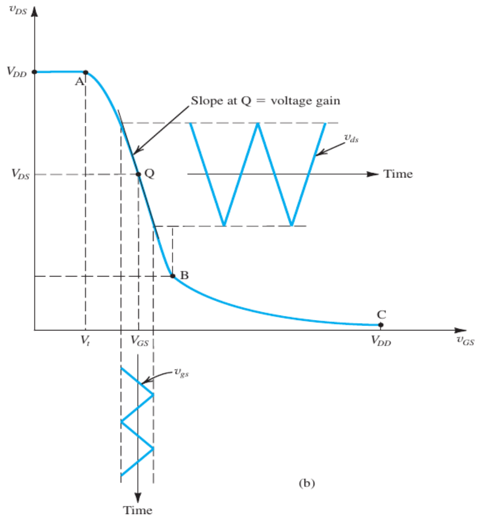


Figure 5.31 Graphical construction to determine the voltage transfer characteristic of the amplifier in Fig. 5.29(a).

- Consider the VTC shown in figure
    - here the value of R_D is fixed
        - the only remaining variable is the value of V_{GS}
        - Note that the slope increases as we move closer to point B
            - thus higher gain is achieved by locating Q as close to B as possible
        - However the closer Q is to the boundary point B,
            - the smaller the allowable magnitude of negative signal swing



- to decide on the value of R_D, $i_D - v_{DS}$ plane is useful
    - here two load lines are shown which result in two exreme bias points
        - Point Q_1 is too close to V_{DD}
            - resulting in a severe constaint on the positive signal swing of v_{ds}
            - Exceeding the allowable +ve maximum will result in positive peaks of the signal being cliiped off,
            - since the MOSFET will turn off for the part of each cycle near the+ve peak
            - we say the circuit doesnot have sufficient

“headroom”

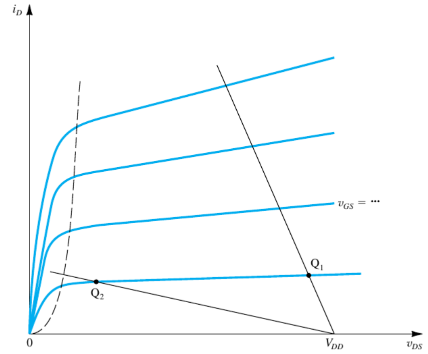


Figure 5.33 Two load lines and corresponding bias points. Bias point Q_1 does not leave sufficient room for positive signal swing at the drain (too close to V_{DD}). Bias point Q_2 is too close to the boundary of the triode region and might not allow for sufficient negative signal swing.

- Point Q_2 is very close to the boundary of the triode region,
  - thus severely limiting the allowable negative signal swing of v_{ds}
    - Exceeding this limit results in the transistor entering the triode region,
      - for part of each cycle near the negative peaks,
      - resulting in a distorted output signal
      - we say the circuit doesnot have sufficient “legroom”

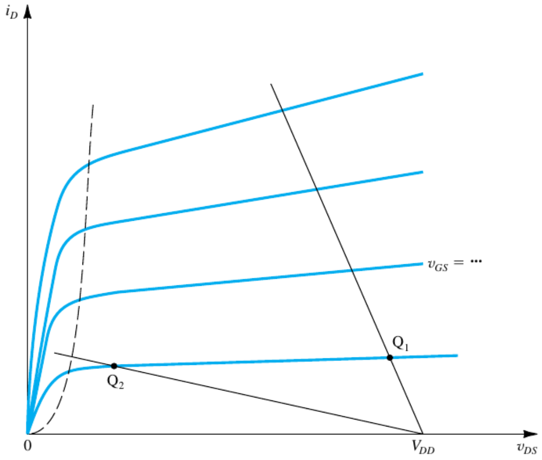


Figure 5.33 Two load lines and corresponding bias points. Bias point Q_1 does not leave sufficient room for positive signal swing at the drain (too close to V_{DD}). Bias point Q_2 is too close to the boundary of the triode region and might not allow for sufficient negative signal swing.