Lecture 8a

EE-215 Electronic Devices and Circuits

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Biasing in MOS Amplifier Circuits

- we have already determined
    - In the design of a MOS amplifier circuit,
        - it is essential to establish an appropriate dc operating point (or Q point or bias point) for the MOSFET
        - This step is known as biasing or bias design
    - An appropriate bias point or dc operating point is characterized by
        - a stable and predictable dc drain current I_D and
        - by a dc drain-to-source voltage V_{DS} that ensures operation in the saturation region for all expected input signal levels

Biasing by Fixing V_{GS}

- The simplest way to bias a MOSFET is to fix its gate-to-source voltage, V_{GS}
    - to the value that is required for the desired I_D
    - This voltage can be easily derived from the power-supply V_{DD}
        - by using an appropriate voltage divider
    - however, this way of biasing a MOSFET is not a good approach
        - because practically there are always some variations in V_t, C_{ox} among the devices of same type
    - As $I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_t)^2$
        - if V_t , C_{ox} of two devices is different
        - $=\Rightarrow I_D$ will be different for the same value of V_{GS}
- also, V_t and μ_n are temperature dependent, and if we fix the value of V_{GS},
    - the drain current I_D will become very temperature dependent
    - thus for the fixed value of V_{GS}, the resultant spread
        - in the value of drain current can be substantial
            - ($\because$ of change in V_t , C_{ox} , μ_n among the devices of same type)

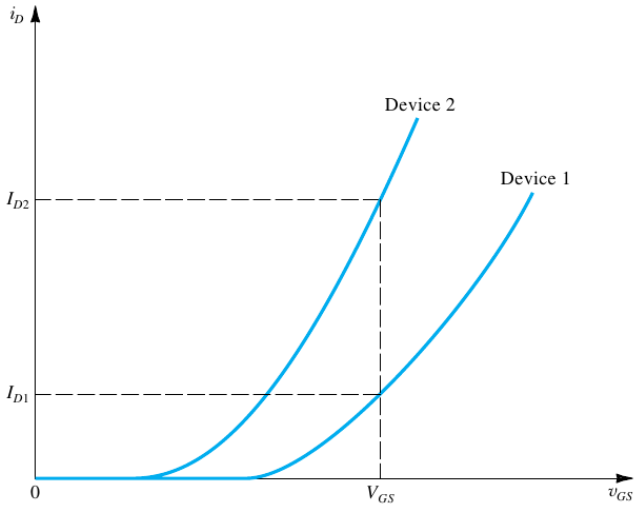
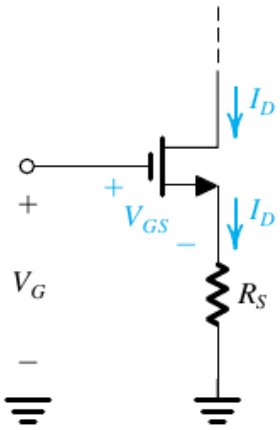


Figure 5.51 The use of fixed bias (constant V_{GS}) can result in a large variability in the value of I_D. Devices 1 and 2 represent extremes among units of the same type.

Biasing by Fixing V_G and Connecting a Resistance in the Source

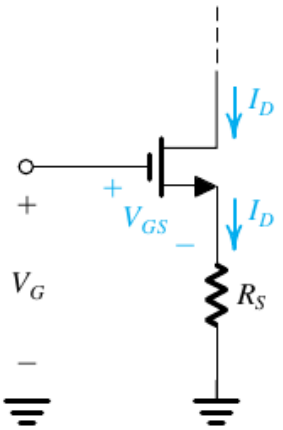
- An effective biasing technique for discrete MOSFET circuits,
  - consists of fixing the dc voltage at the gate V_G
    - and connecting a resistance in the source lead
  - By KVL , $V_G = V_{GS} + I_D R_S \Longrightarrow I_D = \frac{V_G - V_{GS}}{R_S}$
  - from this relation, if V_G is much greater than V_{GS}
    - $\Longrightarrow I_D$ will be mostly determined by V_G and R_S
    - even when V_G is not much larger than V_{GS}, resistor R_S
      - provides a negative feedback which acts to stabilize the value of the bias current I_D



(a)

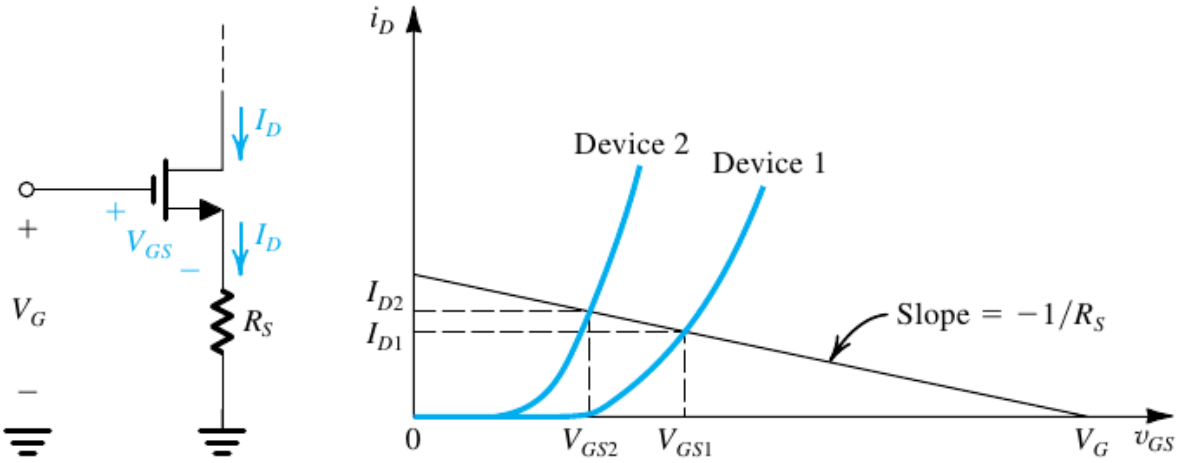
- $V_G = V_{GS} + I_D R_S \Longrightarrow I_D = \frac{V_G - V_{GS}}{R_S}$
  - even when V_G is not much larger than V_{GS}, resistor R_S
    - provides a negative feedback which acts to stabilize the value of the bias current I_D
    - negative feedback here, means that if I_D increases for any reason,
      - the equation ($V_G = V_{GS} + I_D R_S$) indicates that since V_G is a constant,

- V_{GS} will have to decrease. this in turn results in a decrease in I_D



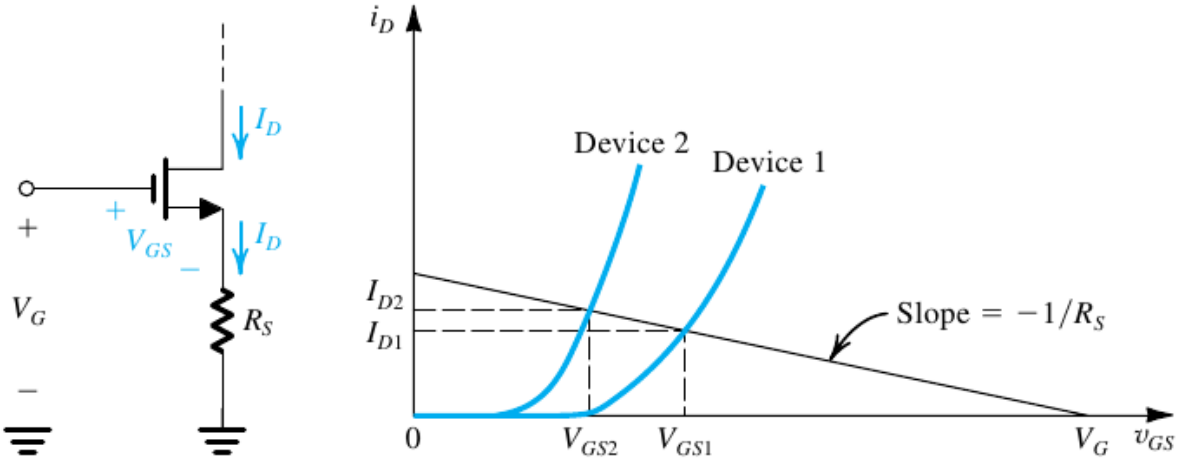
(a)

- Thus the purpose of R_S is to keep I_D as constant as possible



(a) (b)

- here $i_D - v_{GS}$ characteristics for two devices that represent the extremes of a batch of MOSFETs, are shown
- The straight line, (superimposed on the device characteristics), represents the constraint imposed by the bias circuit
  - i.e. $V_G = V_{GS} + I_D R_S$



(a) (b)

- The intersection of this straight line ($V_G = V_{GS} + I_D R_S$) with the $i_D - v_{GS}$ characteristic curve
  - provides the coordinates (I_D, V_{GS}) of the bias point.

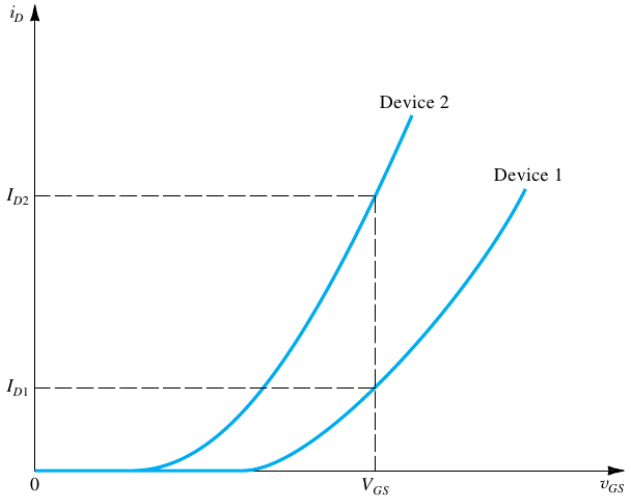
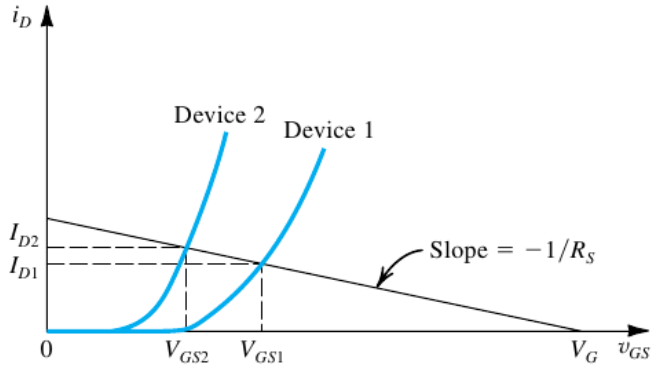
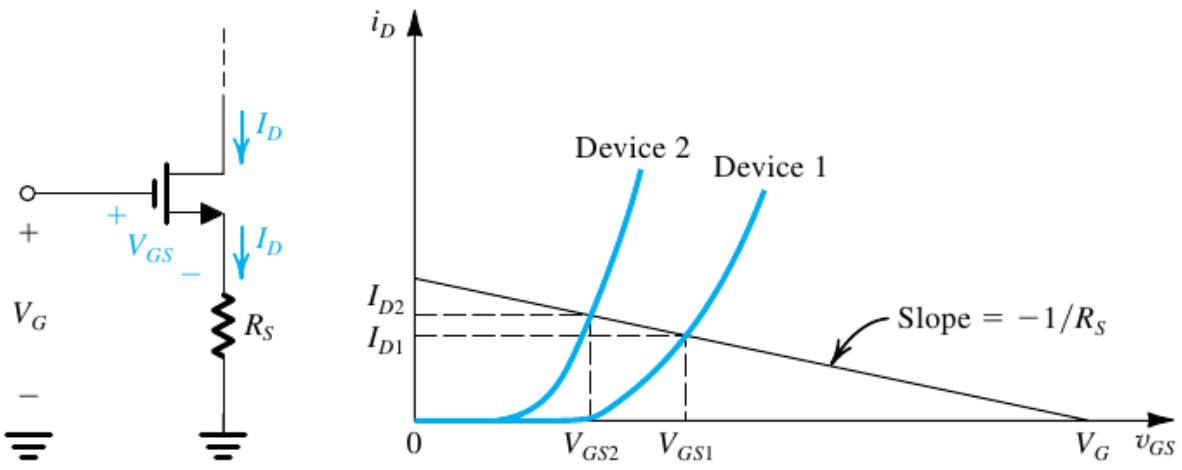


Figure 5.51 The use of fixed bias (constant V_{GS}) can result in a large variability in the value of I_D. Devices 1 and 2 represent extremes among units of the same type.



(b)

- note that compared to the case of fixed V_{GS} (left fig),
  - here (right fig) the variation in I_D is much smaller

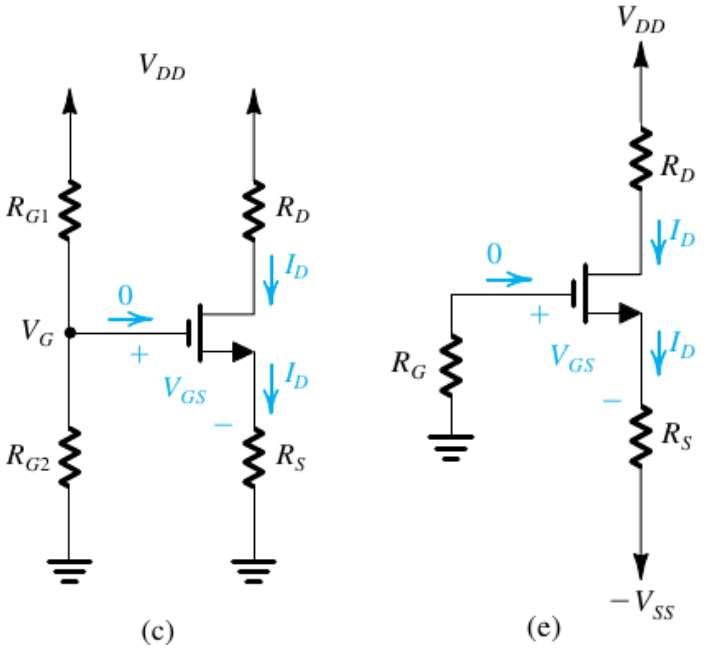


(a) (b)

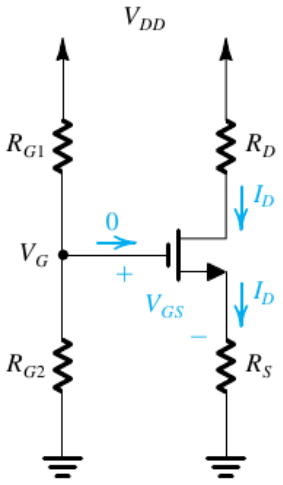
- Note that the variation in I_D decreases as V_G and R_S are made larger
- (i.e. the bias line is less steep when V_G and R_S are larger)

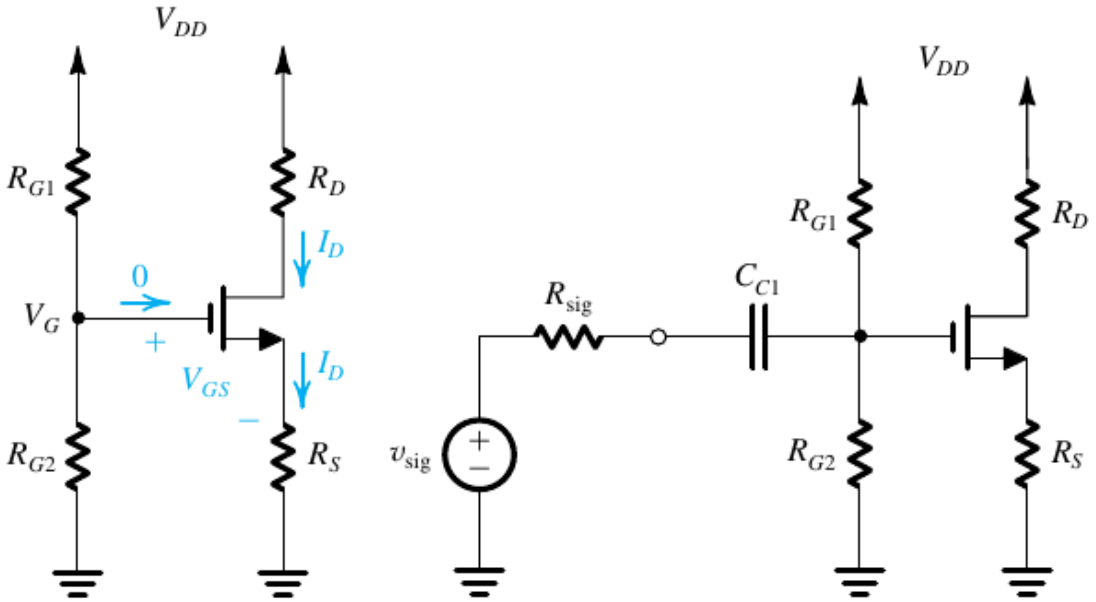
- Two possible practical discrete implementations of this bias scheme are

shown in fig

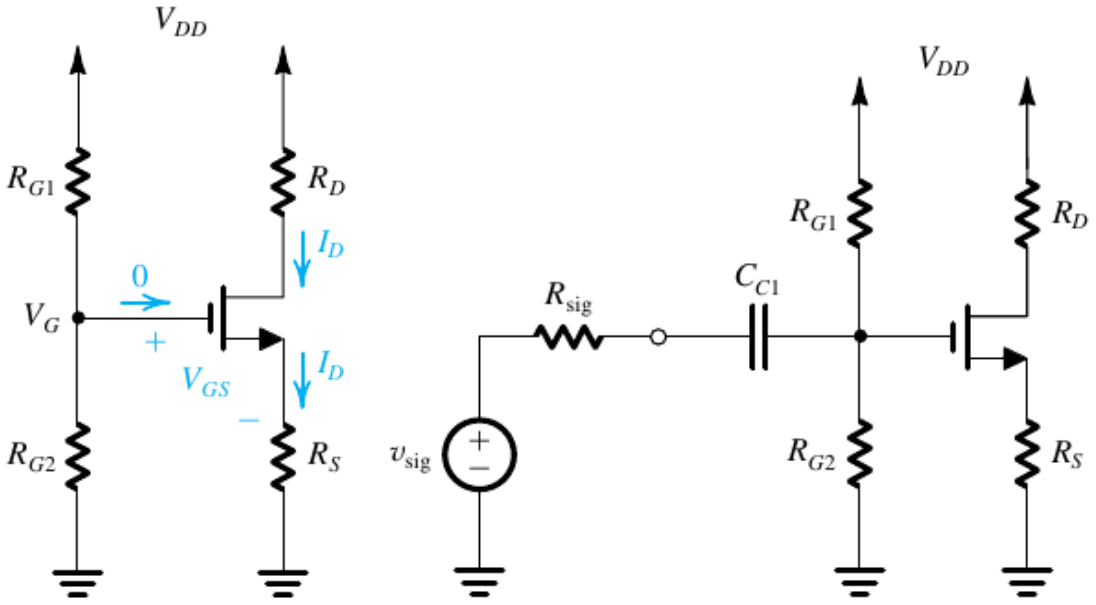


- here just one power supply V_{DD} is required
  - V_G is derived using a voltage divider (R_{G1}, R_{G2})
    - As $I_G = 0$, R_{G1} and R_{G2} can be selected to be very large (usually in Mega ohms range)
    - this allows the MOSFET to present a large R_{in} to the signal source
      - that can be connected to the gate through a coupling capacitor



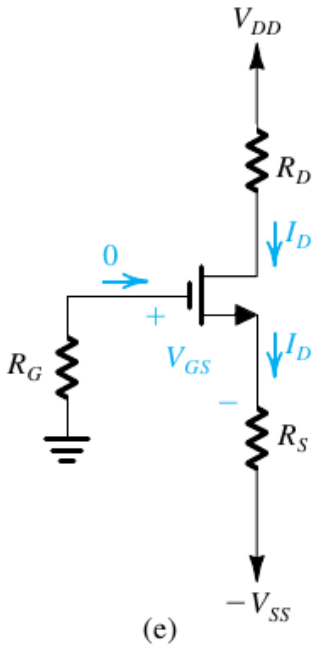


- (c) (d)
  - here capacitor C_{C1} blocks dc and thus enables us to couple
    - the signal v_{sig} to the amplifier input without disturbing the MOSFET bias point



- (c) (d)
  - The value of C_{C1} should be selected large enough to
    - approximate a short circuit at all signal frequencies of interest
- if two power supplies are available, a relatively simpler biasing scheme can be used
  - as gate current is zero $= \Rightarrow V_G = 0$
    - by KVL, $V_G = V_{GS} + I_D R_S + (-V_{SS})$
      - $0 = V_{GS} + I_D R_S - V_{SS} = \Rightarrow V_{SS} = V_{GS} + I_D R_S$
    - Note that this relation is of the same form as the relation for the previous circuit ($V_G = V_{GS} + I_D R_S$), if V_G is replaced by V_{SS}

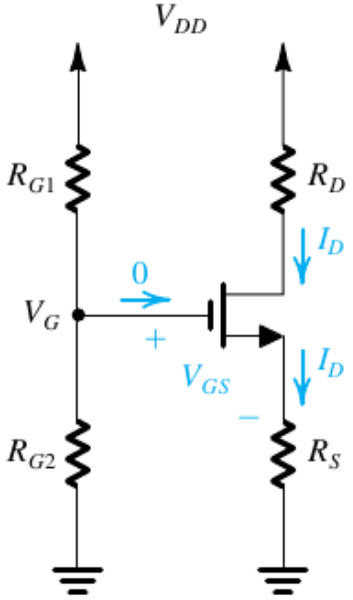
- Note that R_G establishes a dc ground at the gate
  - and presents a high input resistance to a signal source
  - which may be connected to the gate through a coupling capacitor



(e)

Example 5.12

- It is required to design the circuit of Fig. 5.52(c) to establish a dc drain current $I_D = 0.5mA$. The MOSFET is specified to have $V_t = 1V$ and $k_n'(W/L) = 1mA/V^2$. For simplicity, neglect the channel-length modulation effect (i.e., assume $\lambda = 0$). Use a power-supply $V_{DD} = 15V$. Calculate the percentage change in the value of I_D obtained when the MOSFET is replaced with another unit having the same $k_n'(W/L)$ but $V_t = 1.5V$.

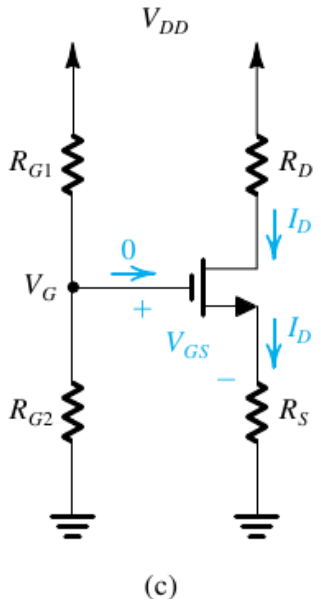


(c)

Solution:

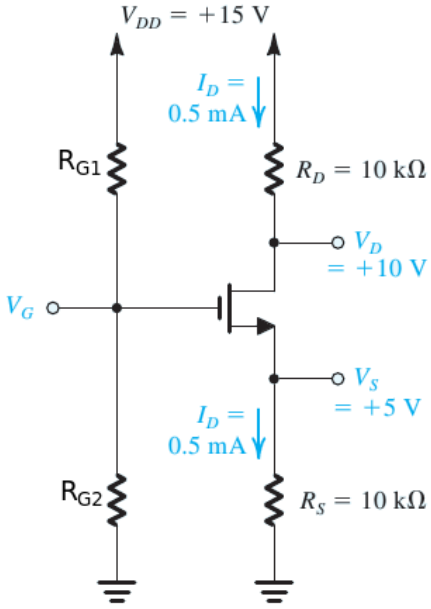
- As a rule of thumb, this biasing circuit can be designed by

- selecting R_D and R_S to provide one-third of the V_{DD}
  - as a voltage drop across each of the
    - R_D , the transistor (i.e. V_{DS}) and R_S
  - i.e. $I_D R_D = V_{DS} = I_D R_S = \frac{1}{3} V_{DD} = 5V$
    - $= \Rightarrow V_D = 10V$, $V_S = 5V$
  - here 1st two conditions ($I_D R_D = V_{DS} = \frac{1}{3} V_{DD}$) will ensure enough signal swing
  - 3rd condition ($I_D R_S = \frac{1}{3} V_{DD}$) will ensure bias point stability

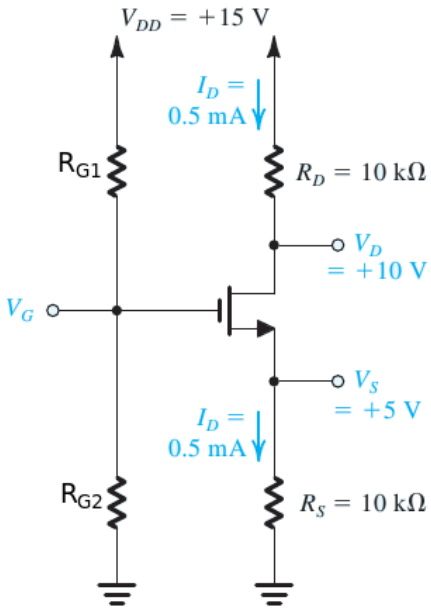


(c)

- here $I_D = 0.5mA$, $V_{DD} = 15V$, $V_t = 1V$, $k_n'(W / L) = 1mA/V^2$, $\lambda = 0$
  - as $I_D R_D = I_D R_S = 5V$, $I_D = 0.5mA$
    - $= \Rightarrow R_D = R_S = \frac{5}{I_D} = \frac{5}{0.5m} = 10k\Omega$
    - to determine V_{GS}
      - $I_D = 0.5mA = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2$
      - $0.5mA = \frac{1}{2} (1m) (V_{GS} - 1)^2$
      - $1 = (V_{GS} - 1)^2 = \Rightarrow (V_{GS} - 1) = \sqrt{1} = \pm 1$
      - $(V_{GS} - 1) = 1 \because V_{OV}$ cannot be -ve if $I_D = 0.5mA$
      - $V_{GS} = 2V$

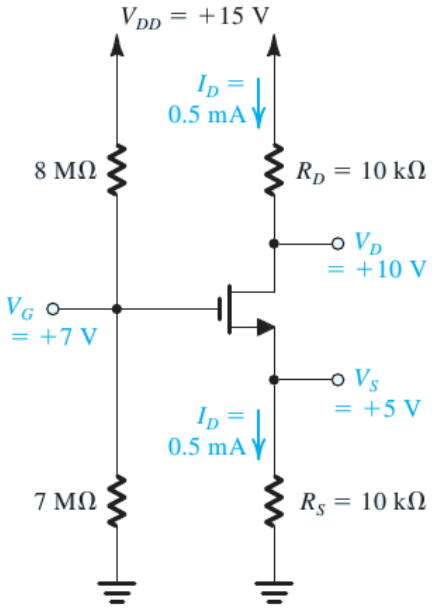


- here $I_D = 0.5mA$, $V_{DD} = 15V$, $V_t = 1V$, $k_n'(W / L) = 1mA/V^2$, $\lambda = 0$
    - $V_{GS} = 2V$
        - $= \Rightarrow V_G - V_S = 2V = V_G - 5V \because V_S = 5V$
            - $V_G - 5 = 2 = \Rightarrow V_G = 7V$
        - now to determine R_{G1} and R_{G2}
            - for $I_{RG1} = I_{RG2} = 1\mu A$
            - $= \Rightarrow R_{G2} = \frac{V_G}{I_{RG2}} = \frac{7}{1\mu} = 7M\Omega$
        - also by ohms law
            - $V_{DD} = I_{RG1}(R_{G1} + R_{G2})$
            - $15 = 1\mu(R_{G1} + 7M)$
            - $R_{G1} + 7M = 15M = \Rightarrow R_{G1} = 8M\Omega$

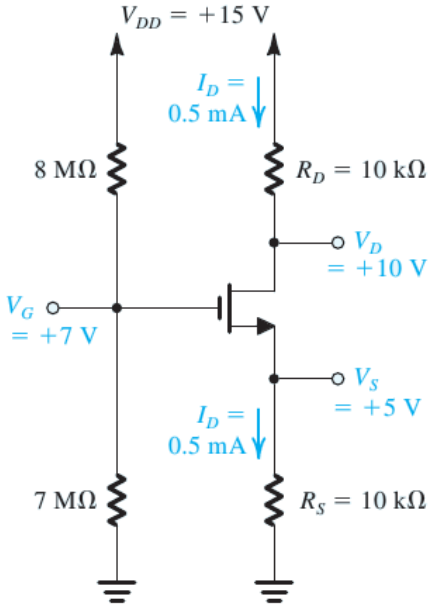


- here $I_D = 0.5mA$, $V_{DD} = 15V$, $V_t = 1V$, $k_n'(W / L) = 1mA/V^2$, $\lambda = 0$

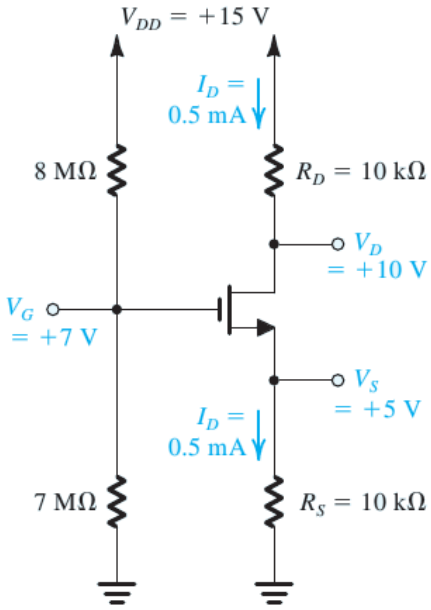
- Note that the dc voltage at the drain is +10V and $V_{DD} = +15V$
  - $= \Rightarrow$ maximum +ve signal swing $= 15 - 10 = 5V$
  - for maximum -ve signal swing
    - $V_{DS} \geq V_{GS} - V_t = 2 - 1 = 1V$
    - $V_{DS} \geq 1V$
    - here $V_{DS} = 5V$
    - $= \Rightarrow$ maximum -ve signal swing is -4V (i.e. down to $V_{GS} - V_t = 1V$)



- if now the MOSFET is replaced with another having $V_t = 1.5V$, $k_n'(W / L) = 1mA/V^2$, $\lambda = 0$
  - the new I_D is
    - $I_D = \frac{1}{2} k_n' \left(W / L\right)(V_{GS} - V_t)^2$
      - $I_D = \frac{1}{2} \left(1m\right)(V_{GS} - 1.5)^2 = 0.5m(V_{GS} - 1.5)^2$
    - As $V_G = V_{GS} + I_D R_S$
      - $= \Rightarrow 7 = V_{GS} + I_D(10k)$
      - or $I_D = \frac{7 - V_{GS}}{10k}$
    - eliminating I_D from the above two equations
      - $I_D = 0.5m(V_{GS} - 1.5)^2 = \frac{7 - V_{GS}}{10k}$
      - $(V_{GS} - 1.5)^2 = \frac{7 - V_{GS}}{5}$



- $(V_{GS} - 1.5)^2 = \frac{7 - V_{GS}}{5}$
  - $V_{GS}^2 + (1.5)^2 - 2\left(V_{GS}\right)\left(1.5\right) = \frac{7 - V_{GS}}{5}$
    - $V_{GS}^2 + 2.25 - 3V_{GS} = \frac{7 - V_{GS}}{5}$
      - $5V_{GS}^2 + 11.25 - 15V_{GS} = 7 - V_{GS}$
      - $5V_{GS}^2 + 4.25 - 14V_{GS} = 0$
      - $5V_{GS}^2 - 14V_{GS} + 4.25 = 0$
    - $= \Rightarrow V_{GS} = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} = \frac{14 \pm \sqrt{14^2 - 4(5)(4.25)}}{2(5)}$
      - $V_{GS} = \frac{14 \pm \sqrt{111}}{10} = 2.4536\,,\, 0.34643$
      - As $V_t = 1.5V$ and as I_D is not zero $= \Rightarrow V_{GS}$ can not be equal to 0.34643V
      - $= \Rightarrow V_{GS} = 2.4536V$



- As $I_D = \frac{7-V_{GS}}{10k} = \Rightarrow I_D = \frac{7-2.4536}{10k} = 0.45464mA$

- $I_D = 0.5mA$ when initially $V_t = 1V$
  - and $I_D = 0.45464mA$ when $V_t = 1.5V$
  - $= \Rightarrow$
    - the change in I_D is
    - $\Delta I_D = 0.45464m - 0.5m = -0.04536mA$
  - thus the %age change is
    - $\frac{\Delta I_D}{I_D} \times 100 = \frac{-0.04536m}{0.5m} \times 100 = -9.072\%$

Exercise 5.33

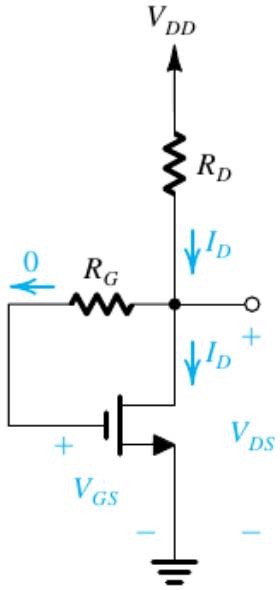
- Consider the MOSFET in Example 5.12 when fixed-V_{GS} bias is used. Find the required value of V_{GS} to establish a dc bias current $I_D = 0.5mA$. Recall that the device parameters are $V_t = 1V$, $k_n'\left(W / L\right) = 1mA/V^2$, and $\lambda = 0$. What is the percentage change in I_D obtained when the transistor is replaced with another having $V_t = 1.5V$?

Solution:

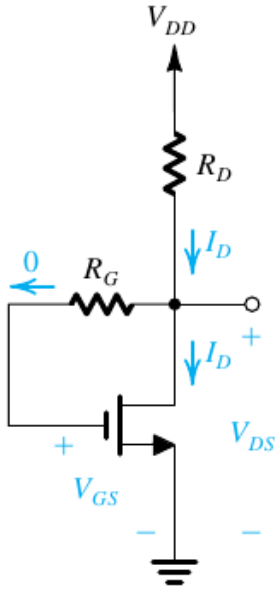
- here $I_D = 0.5mA$
  - $I_D = 0.5m = \frac{1}{2}k_n'\frac{W}{L}(V_{GS} - V_t)^2 = \Rightarrow 0.5m = \frac{1}{2}\left(1m\right)(V_{GS} - V_t)^2$
    - $1 = (V_{GS} - V_t)^2 = \Rightarrow V_{GS} - V_t = 1$ or $V_{GS} = 1 + 1 = 2V$
  - Now if $V_t = 1.5V$
    - $I_D = \frac{1}{2}k_n'\frac{W}{L}(V_{GS} - V_t)^2 = \frac{1}{2}\left(1m\right)(V_{GS} - 1.5)^2$
    - As V_{GS} is fixed to 2V
    - $= \Rightarrow I_D = \frac{1}{2}\left(1m\right)(2 - 1.5)^2 = 0.125mA$
  - $\Delta I_D = 0.125m - 0.5m = -0.375mA$
  - and $\frac{\Delta I_D}{I_D}$ in percentage$= \frac{-0.375m}{0.5m} \times 100 = -75\%$

Biasing Using a Drain-to-Gate Feedback Resistor

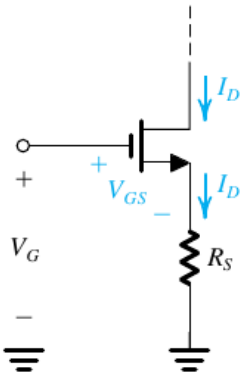
- Another effective discrete-circuit biasing arrangement is possible by
  - connecting a feedback resistor between the drain and the gate
    - here the resistance R_G (typically in mega ohms range) forces
      - the dc voltage at the gate to be equal to that at the drain ($\because I_G = 0$)
      - $= \Rightarrow V_G = V_D$ or $V_{GS} = V_{DS}$
    - by KVL
      - $V_{DD} = I_D R_D + V_{DS}$
      - $V_{DD} = I_D R_D + V_{GS} \because V_{GS} = V_{DS}$
      - or $V_{DD} = V_{GS} + I_D R_D$



- $V_{DD} = V_{GS} + I_D R_D$
  - which is identical in form to the one obtained for the "biasing by fixing V_G and connecting R_S in the source"
  - $V_{DD} = V_{GS} + I_D R_D$



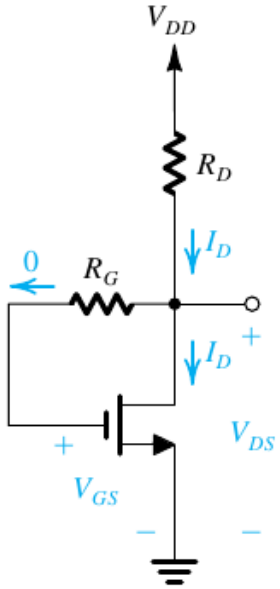
- $V_G = V_{GS} + I_D R_S$



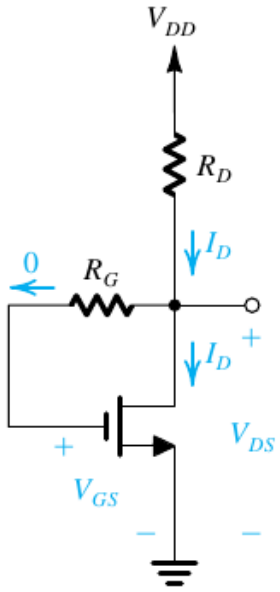
(a)

- $V_{DD} = V_{GS} + I_D R_D$
  - thus, if I_D for some reason changes, say increases, then

- the above equation indicate that V_{GS} must decrease.
  - This decrease in V_{GS} in turn causes a decrease in I_D
- thus the negative feedback provided by R_G works to keep
  - the value of I_D as constant as possible



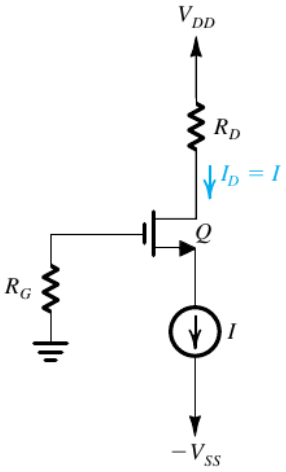
- to use this circuit as a CS amplifier, the input voltage
  - signal can be applied to the gate via a coupling capacitor,
    - so as not to disturb the dc bias condition
    - the amplified output signal at the drain can be coupled to another part
      - of the circuit again via a coupling capacitor



Biasing Using a Constant-Current Source

- Another effective way for biasing a MOSFET is shown in fig and it utilizes a constant-current source
  - here R_G (usually in mega ohms range) establishes a dc ground
    - at the gate and presents a large resistance to an input signal source

        - that can be coupled to the gate via a coupling capacitor
    - resistor R_D establishes an appropriate dc voltage at the drain
        - to allow for the required signal swing while ensuring
        - that the transistor always remains in the saturation region



    - (a)

- the current source I is implemented by the current mirror circuit shown in fig b

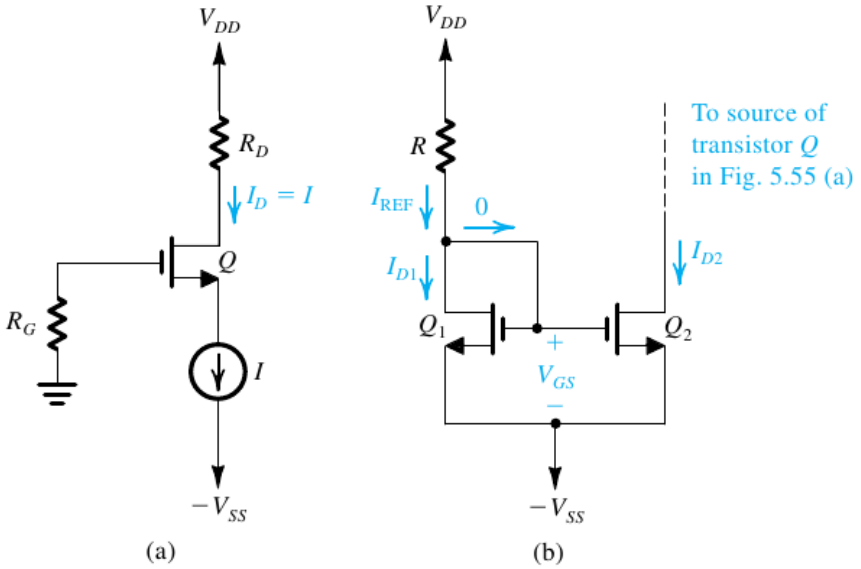
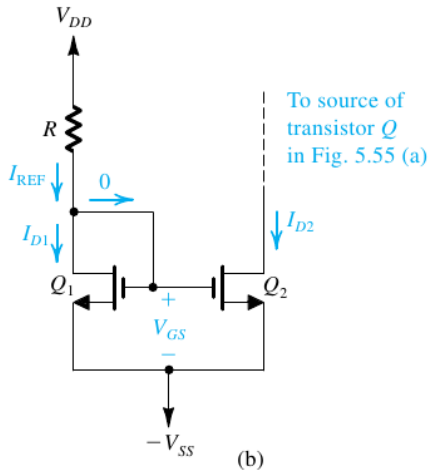
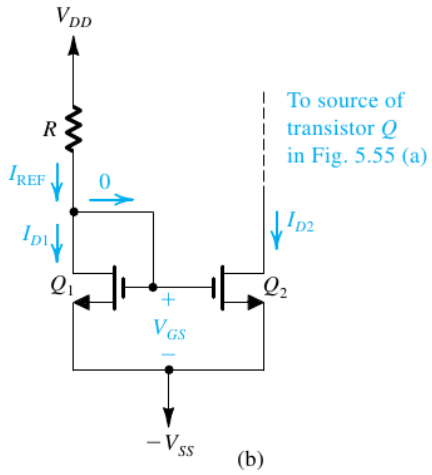


Figure 5.55 **(a)** Biasing the MOSFET using a constant-current source I. **(b)** Implementation of the constant-current source I using a current mirror.

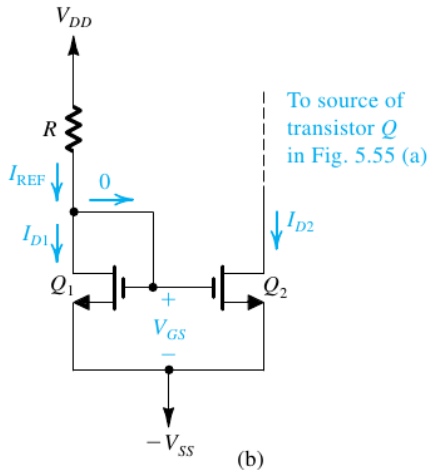
- for the current mirror, the drain of Q_1 is shorted to its gate
    - $= \Rightarrow Q_1$ is operating in the saturation region
        - As for saturation $V_{DS} \geq V_{GS} - V_t$
            - here $V_{DS} = V_{GS} = \Rightarrow 0 \geq -V_t$ which is true
        - neglecting the channel length modulation i.e. $\lambda = 0$
            - $= \Rightarrow I_{D1} = \frac{1}{2} k_n{}' \left(\frac{W}{L}\right)_1 (V_{GS} - V_t)^2$
        - here the drain current I_{D1} is supplied by V_{DD} through R
            - As gate current is zero $= \Rightarrow I_{D1} = I_{REF}$



- By KVL
  - $V_{DD} = I_{REF}R + V_{GS} + (-V_{SS})$
    - or $(V_{DD} + V_{SS}) = V_{GS} + I_{REF}R$ where $I_{REF} = I_{D1}$
    - Note that this equation is of the same form as the one in the previous biasing schemes
      - $= \Rightarrow$the drain current will not change much if Q_1 is replaced by another transistor of same type
    - $I_{REF} = I_{D1} = \frac{(V_{DD}+V_{SS})-V_{GS}}{R}$



- now the transistor Q_2 has the same V_{GS} as Q_1
  - thus if we assume that Q_2 is in saturation
    - $= \Rightarrow I = I_{D2} = \frac{1}{2}k_n'\left(\frac{W}{L}\right)_2(V_{GS} - V_t)^2$
      - or $I_{D2}/\left(\frac{W}{L}\right)_2 = \frac{1}{2}k_n'(V_{GS} - V_t)^2$
    - as V_{GS} , V_t and k_n' are the same for Q_1 and Q_2, and as $I_{D1} = \frac{1}{2}k_n'\left(\frac{W}{L}\right)_1(V_{GS} - V_t)^2$
      - $= \Rightarrow I_{D1}/\left(\frac{W}{L}\right)_1 = \frac{1}{2}k_n'(V_{GS} - V_t)^2$



- $= \Rightarrow I_{D2}/\left(\frac{W}{L}\right)_2 = \frac{1}{2}k_n'(V_{GS} - V_t)^2 = I_{D1}/\left(\frac{W}{L}\right)_1$
  - or $I_{D2}/\left(\frac{W}{L}\right)_2 = I_{D1}/\left(\frac{W}{L}\right)_1$
- or $I_{D2}/\left(\frac{W}{L}\right)_2 = I_{D1}/\left(\frac{W}{L}\right)_1$
  - As $I_{D2} = I$ and $I_{D1} = I_{REF}$
    - $= \Rightarrow I/\left(\frac{W}{L}\right)_2 = I_{REF}/\left(\frac{W}{L}\right)_1$
    - $= \Rightarrow$

$$I = I_{REF}\frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}$$

    - thus I is related to I_{REF} by the ratio of the aspect ratios of Q_1 and Q_2
    - This circuit is known as a current mirror, and is very popular in the design of IC MOS amplifiers