

# EC-310 Microprocessor and Microcontroller Based Design

## Frequency Divider

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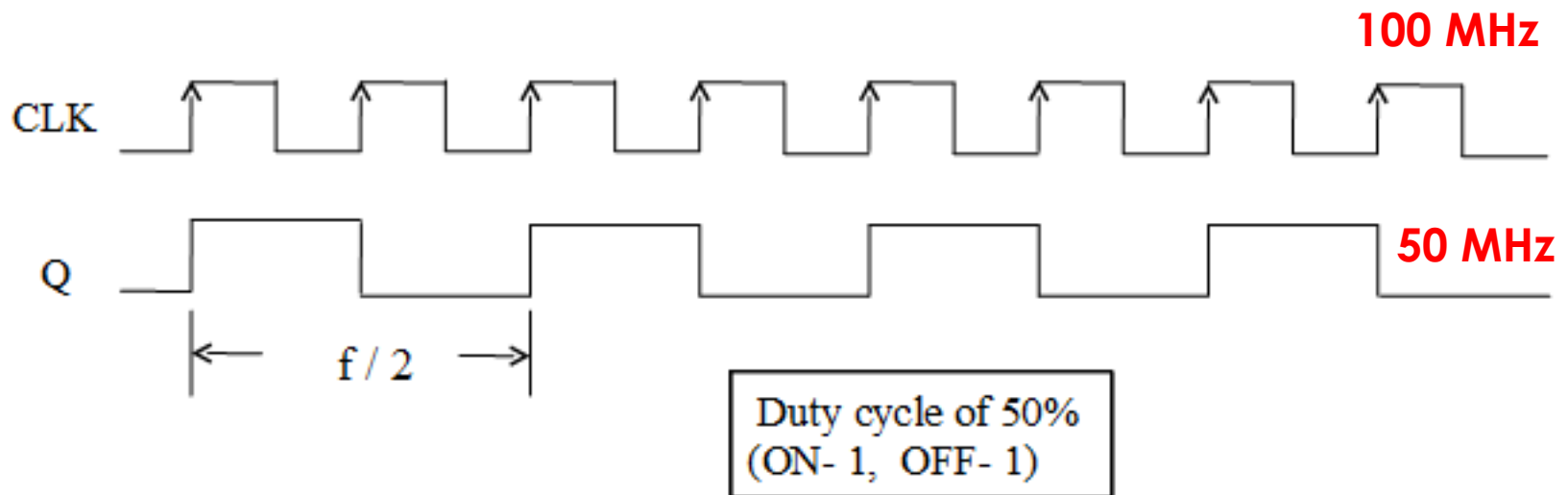
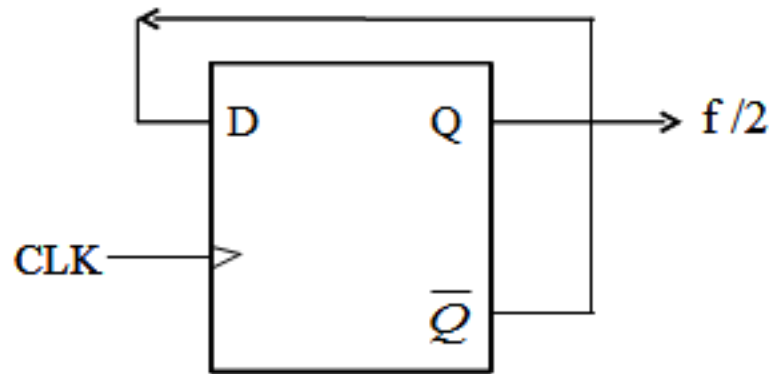
[nazar.abbas@ceme.nust.edu.pk](mailto:nazar.abbas@ceme.nust.edu.pk)

# Divide by N Counter

- ▣ Divide by 3 counter
- ▣ Divide by 8 counter

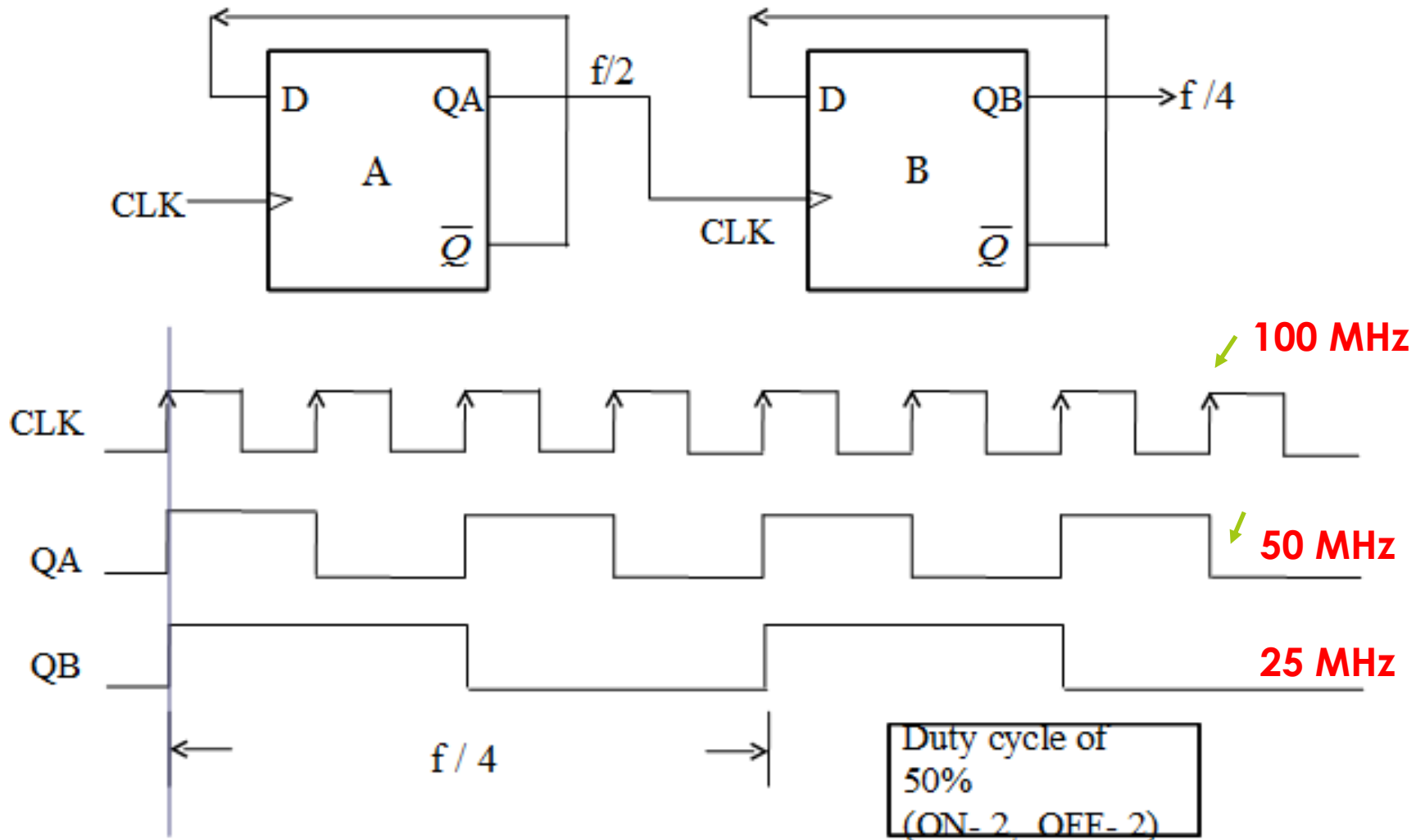
# Divide by N Counter

## Frequency Divide by 2 ( $f/2$ )

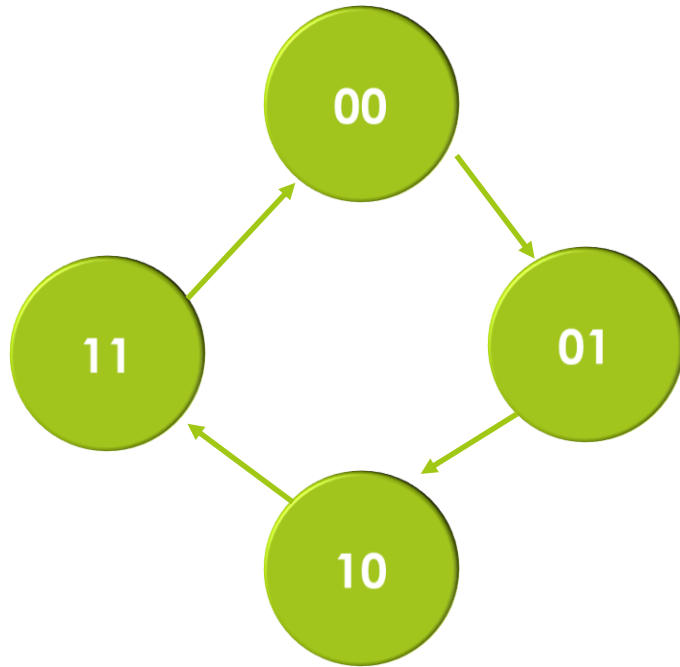


# Frequency Divider

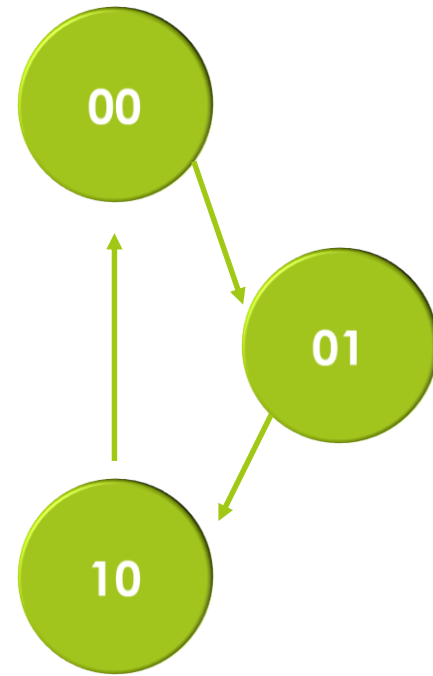
## Frequency Divide by 4 ( $f/4$ )



# Divide-by-3 Counter



Divide by 4



Divide by 3

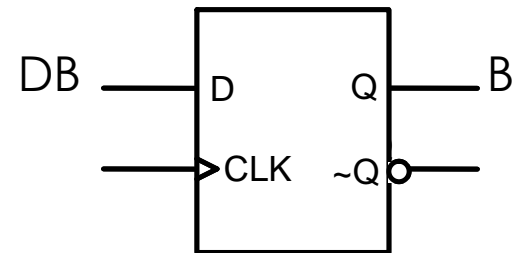
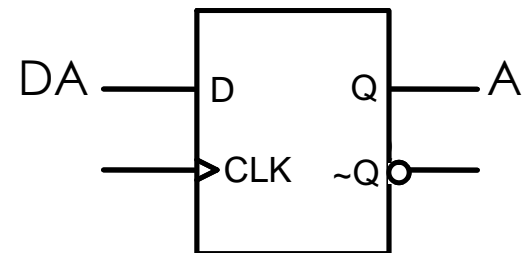
# Divide-by-3 Counter

State	Present state		Next state	
	B	A	$D_B$	$D_A$
<b>s0</b>	0	0	0	1
<b>s1</b>	0	1	1	0
<b>s2</b>	1	0	0	0

A state-transition table

# Divide-by-3 Counter

State	Present state		Next state	
	B	A	$D_B$	$D_A$
<b>s0</b>	0	0	0	1
<b>s1</b>	0	1	1	0
<b>s2</b>	1	0	0	0



# Divide-by-3 Counter

State	Present state		Next state	
	B	A	$D_B$	$D_A$
<b>s0</b>	0	0	0	1
<b>s1</b>	0	1	1	0
<b>s2</b>	1	0	0	0

		A	
		0	1
B	0	1	
	1		

$$D_A = \overline{A}B$$



# Divide-by-3 Counter

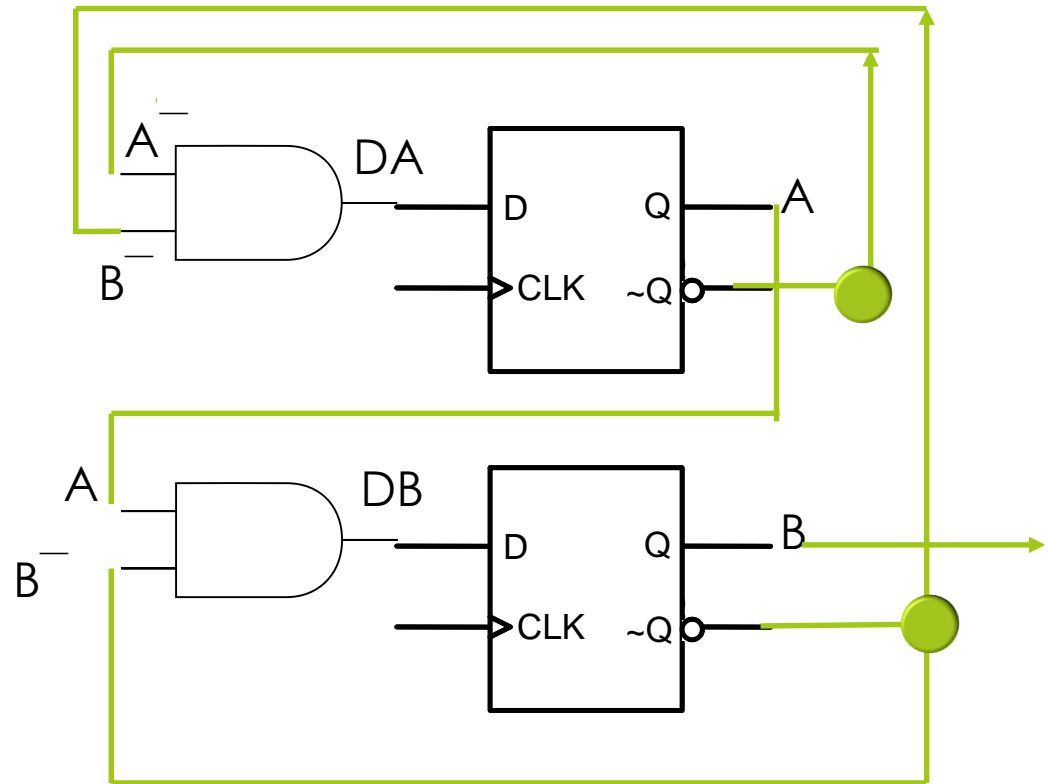
State	Present state		Next state	
	B	A	$D_B$	$D_A$
<b>s0</b>	0	0	0	1
<b>s1</b>	0	1	1	0
<b>s2</b>	1	0	0	0

		A	
		0	1
B	0		
	1	1	

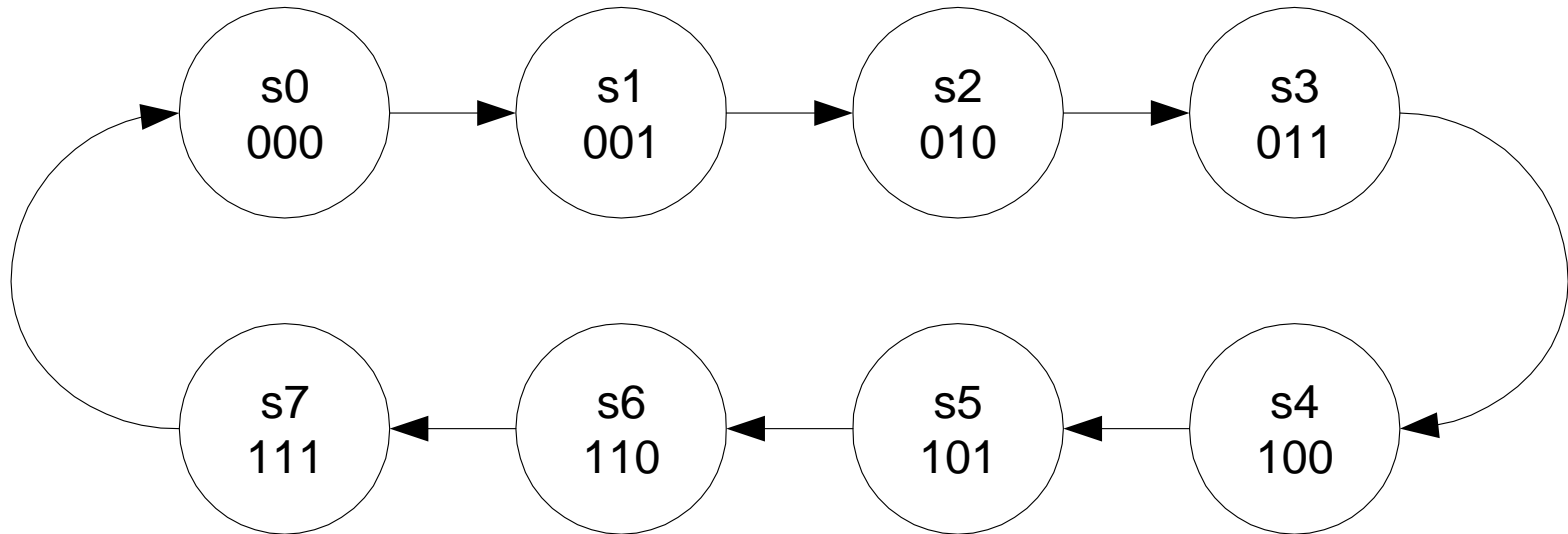
$$D_B = \overline{A}B$$

# Divide-by-3 Counter

A Divide by 3 counter  
Circuit using D Flip-flops



# Divide-by-8 Counter



A state diagram for a divide by 8 counter

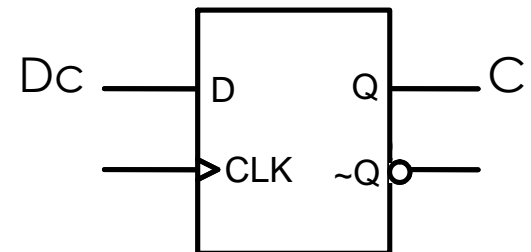
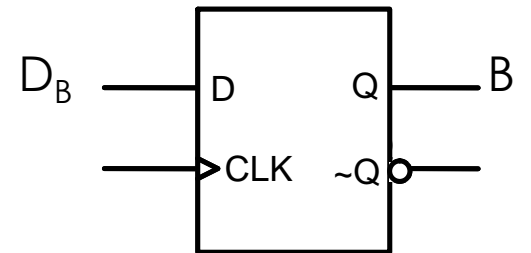
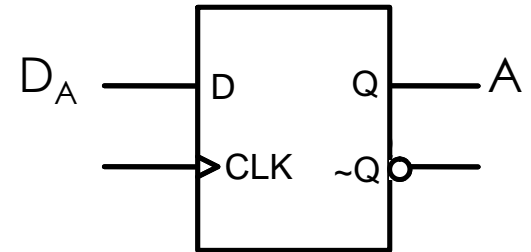
# Divide-by-8 Counter

State	Present state			Next state		
	C	B	A	$D_C$	$D_B$	$D_A$
s0	0	0	0	0	0	1
s1	0	0	1	0	1	0
s2	0	1	0	0	1	1
s3	0	1	1	1	0	0
s4	1	0	0	1	0	1
s5	1	0	1	1	1	0
s6	1	1	0	1	1	1
s7	1	1	1	0	0	0

A state-transition table

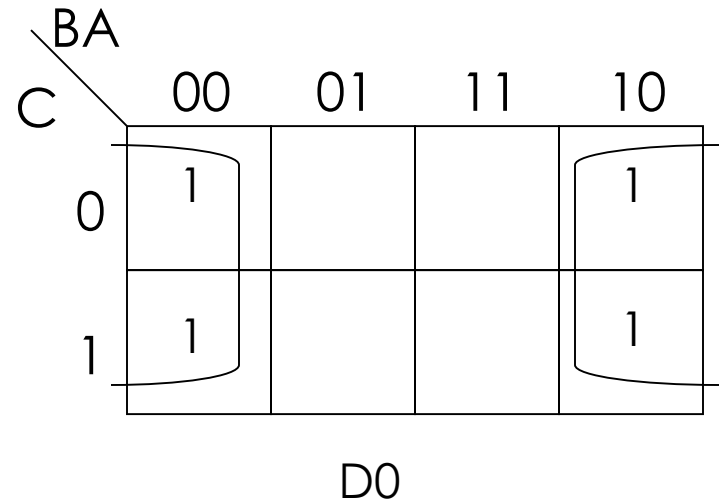
# Divide-by-8 Counter

State	Present state			Next state		
	C	B	A	$D_C$	$D_B$	$D_A$
s0	0	0	0	0	0	1
s1	0	0	1	0	1	0
s2	0	1	0	0	1	1
s3	0	1	1	1	0	0
s4	1	0	0	1	0	1
s5	1	0	1	1	1	0
s6	1	1	0	1	1	1
s7	1	1	1	0	0	0



# Divide-by-8 Counter

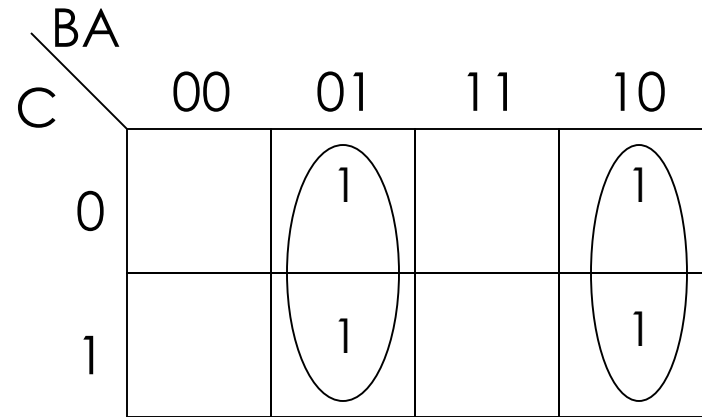
State	Present state			Next state		
	C	B	A	$D_C$	$D_B$	$D_A$
s0	0	0	0	0	0	1
s1	0	0	1	0	1	0
s2	0	1	0	0	1	1
s3	0	1	1	1	0	0
s4	1	0	0	1	0	1
s5	1	0	1	1	1	0
s6	1	1	0	1	1	1
s7	1	1	1	0	0	0



$$D_A = A^-$$

# Divide-by-8 Counter

State	Present state			Next state		
	C	B	A	$D_C$	$D_B$	$D_A$
s0	0	0	0	0	0	1
s1	0	0	1	0	1	0
s2	0	1	0	0	1	1
s3	0	1	1	1	0	0
s4	1	0	0	1	0	1
s5	1	0	1	1	1	0
s6	1	1	0	1	1	1
s7	1	1	1	0	0	0

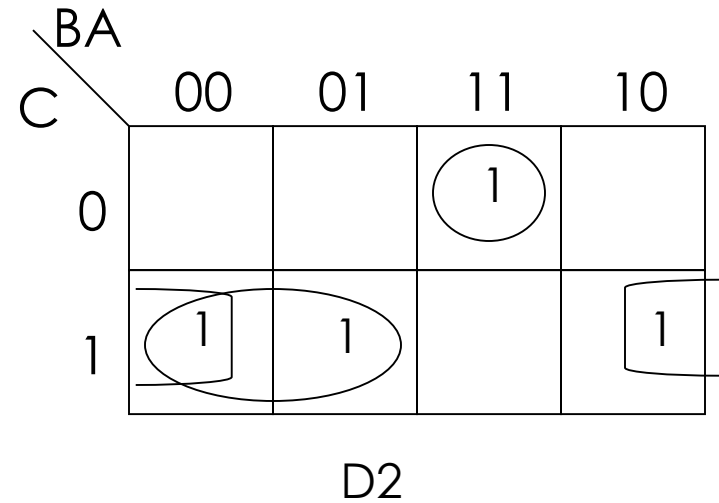


D1

$$D_B = B^- \& A \mid B \& A^-$$

# Divide-by-8 Counter

State	Present state			Next state		
	C	B	A	$D_C$	$D_B$	$D_A$
s0	0	0	0	0	0	1
s1	0	0	1	0	1	0
s2	0	1	0	0	1	1
s3	0	1	1	1	0	0
s4	1	0	0	1	0	1
s5	1	0	1	1	1	0
s6	1	1	0	1	1	1
s7	1	1	1	0	0	0



$$\begin{aligned}
 D_C &= C^- \& B \& A \\
 &| C \& B^- \\
 &| C \& A^-
 \end{aligned}$$



# Divide-by-8 Counter

A Divide by 8 counter  
Circuit using D Flip-flops

